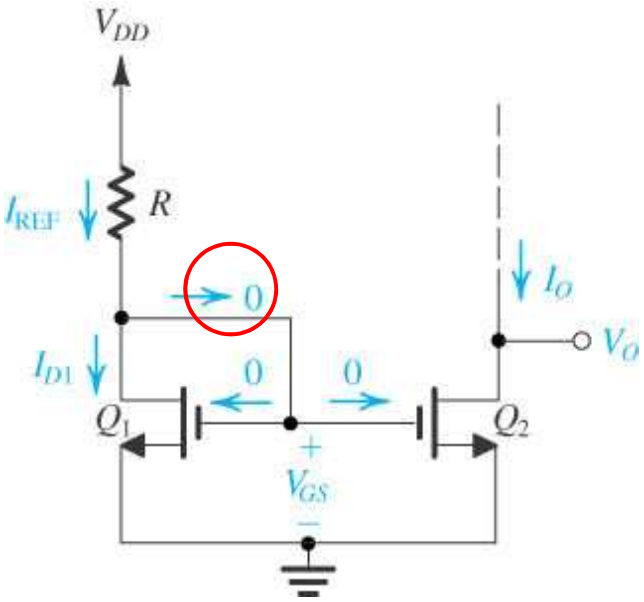
Microelectronic Circuits II

Ch 6 :
Building Blocks of Integrated-Circuit Amplifier

6.4 IC Biasing
6.5 Current-Mirror Circuits

IC Biasing-Current sources, current mirrors & current-steering circuits

- Biasing in integrated-circuit design
  - biasing in the IC by *constant-current source*
  - **current steering** : constant dc current (**reference current**) at one location & *replicated* current source at various other locations
  - utilizes a precision resistor *external* to the chip
  - bias currents *track* each other under changes in power-supply voltage or in temperature
  - circuit building block for *bias* design & *load* element of IC amplifiers
- Basic MOSFET Current Source
  - Drain of Q_1 is shorted to its gate → saturation mode



$$I_{D1} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_{tn})^2$$

- R : outside of IC chip

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

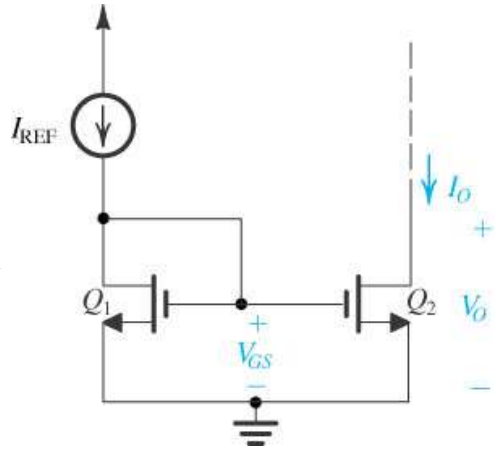
- Q_2 w/ the same V_{GS} as Q_1, assume in saturation

$$I_O = I_{D2} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_{tn})^2$$

Basic MOSFET Current Source

- Relation between I_O and I_{REF}
  - I_O/I_{REF} = ratio of the aspect ratios of the transistor & determined by geometries

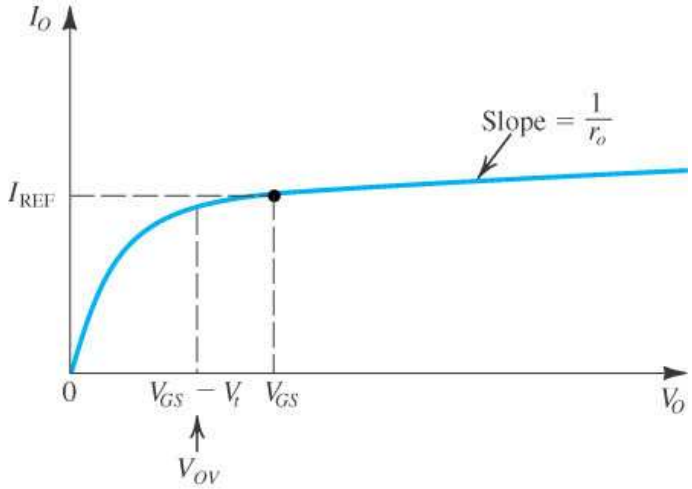
$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$ current gain or current transfer ratio



Basic MOSFET current mirror

- **Current mirror** : identical Q_1 & Q_2 → $I_O = I_{REF}$
  replicates or mirrors the reference current in the output terminal

- Effect of V_O on I_O
  - condition for Q_2 saturation $V_O \geq V_{GS} - V_t$ $V_O \geq V_{OV}$
  - channel length modulation effect
    * I_O at $Q_2 = I_{REF}$ at Q_1 at the same V_{DS} (V_O=V_{GS})
    * if V_O ↑, then I_O ↑ by the incremental output resistance r_{o2} of Q_2



* Finite output resistance R_o of the current mirror

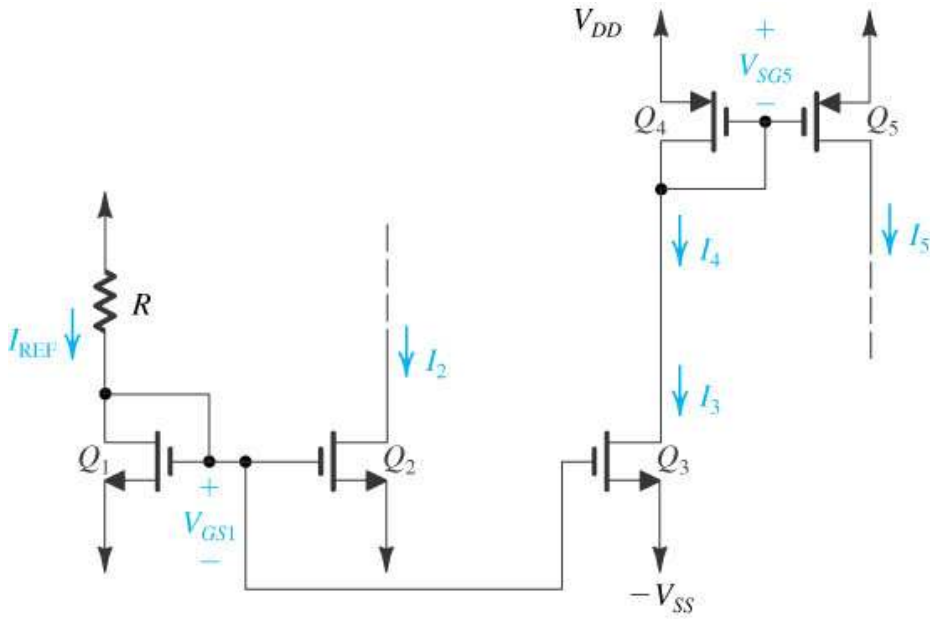
$$R_o \equiv \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O}$$

V_{A2} : Early voltage of Q_2

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF}\left(1 + \frac{V_O - V_{GS}}{V_{A2}}\right)$$

MOS Current-Steering Circuits

- Current-steering circuit
  - constant currents are *replicated* for the various amplifier stages in an IC



- I_{REF} by Q_1 & R
- Q_1, Q_2 & Q_3 → *two-output current mirror*

$$I_2 = I_{REF}\frac{(W/L)_2}{(W/L)_1} \qquad I_3 = I_{REF}\frac{(W/L)_3}{(W/L)_1}$$

- Saturation region at Q_2 & Q_3

$$V_{D2}, V_{D3} \geq -V_{SS} + V_{GS1} - V_{tn}$$

$$\boldsymbol{V_{D2}, V_{D3} \geq -V_{SS} + V_{OV1}}$$

drains of Q_2 & Q_3 must remain higher than $-V_{SS}$ by at least the overdrive voltage (0.1~0.3V)

- current mirror by PMOS Q_4 & Q_5

$$\boldsymbol{I_5 = I_4\frac{(W/L)_5}{(W/L)_4}} \qquad \textit{where, } I_4 = I_3 \qquad \boldsymbol{V_{D5} \leq V_{DD} - |V_{OV5}|} \qquad \text{to keep } Q_5 \text{ in saturation}$$

Q_2 *pulls* its current I_2 from a load → **current sink**

Q_5 *pushes* its current I_5 into a load → **current source**

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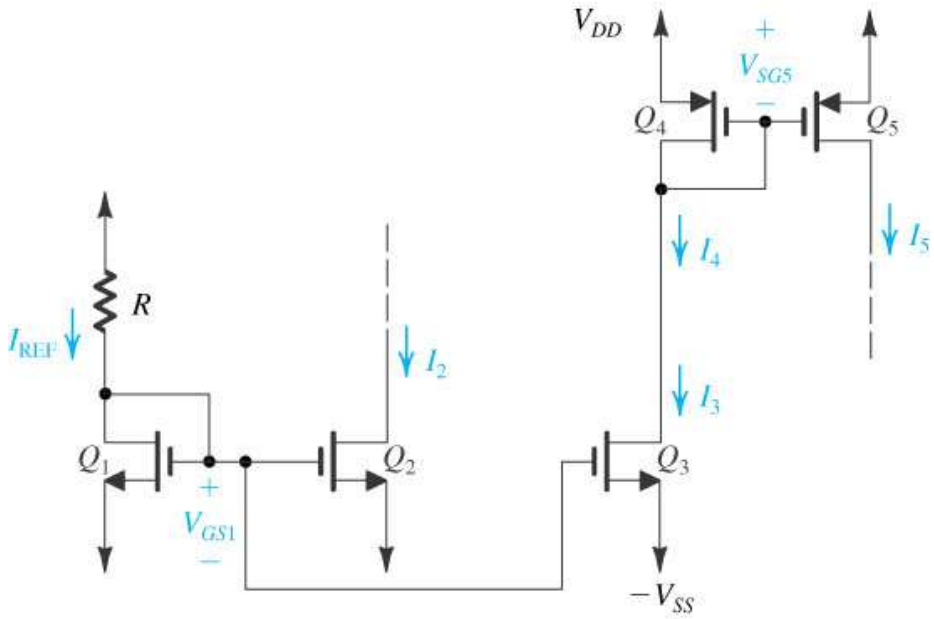

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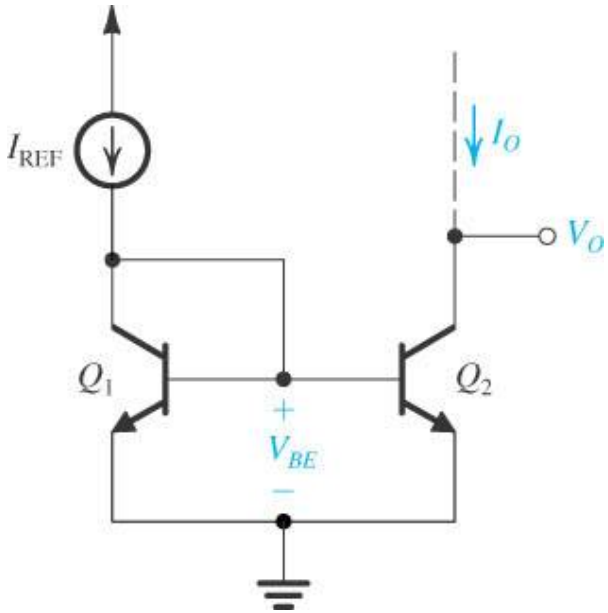
BJT Circuits

- Basic BJT current mirror
  - nonzero base current of the BJT (or, finite β) → *error* in the current transfer ratio (*CTR*)
  - *CTR* by the *relative* areas of the emitter-base junctions of Q_1 & Q_2



$$I_C = I_S e^{V_{BE}/V_T}$$
$$I_C = \alpha I_E \quad I_C = \beta I_B$$

- 1st case : sufficiently high β , neglected I_B
  → I_{REF} passes Q_1 → V_{BE} of Q_1 = V_{BE} of Q_2
  → if $Q_1 = Q_2$, same *EBJ* area & scale current I_S

$$\boldsymbol{I_O = I_{REF}}$$

: active mode at Q_2 :: $V_O > 0.3\text{V} + V_E$ of Q_2

→ area of the *EBJ* of Q_2 is *m* times that of Q_1

$$\boldsymbol{I_O = mI_{REF}}$$

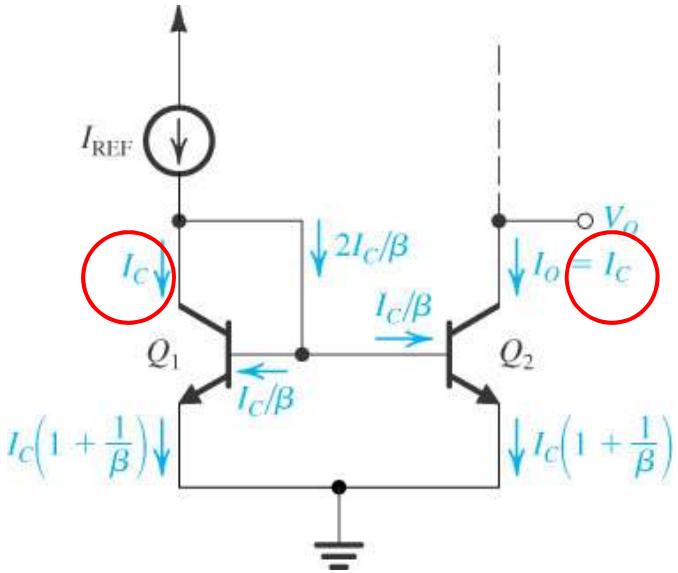
- Current transfer ratio

$$\frac{\boldsymbol{I_O}}{\boldsymbol{I_{REF}}} = \frac{\boldsymbol{I_{S2}}}{\boldsymbol{I_{S1}}} = \frac{\boldsymbol{Area\ of\ EBJ\ of\ Q_2}}{\boldsymbol{Area\ of\ EBJ\ of\ Q_1}}$$

If the area ratio *m* is an integer, one can think of Q_2 as equivalent to *m* transistors, each matches to Q_1 and connected in parallel

BJT Circuits

- 2nd case : effect of finite β on the *CTR*
  - case of *CTR* is unity: Q_1 & Q_2 are matched and same V_{BE} → equal collector currents
  - node equation at the collector of Q_1



$$I_{REF} = I_C + 2I_C/\beta = I_C\left(1+\frac{2}{\beta}\right)$$

since $I_O = I_C$, the *CTR* is

$$\frac{I_O}{I_{REF}} = \frac{I_C}{I_C\left(1+\frac{2}{\beta}\right)} = \boxed{\frac{1}{1+\frac{2}{\beta}}} \qquad \frac{I_O}{I_{REF}} = \frac{m}{1+\frac{m+1}{\beta}}$$

When $I_{S2} = mI_{S1}$

as β → inf. , I_O/I_{REF} → unity

β = 100 results in a 2% error in the *CTR*

- BJT mirror has a finite output resistance R_o

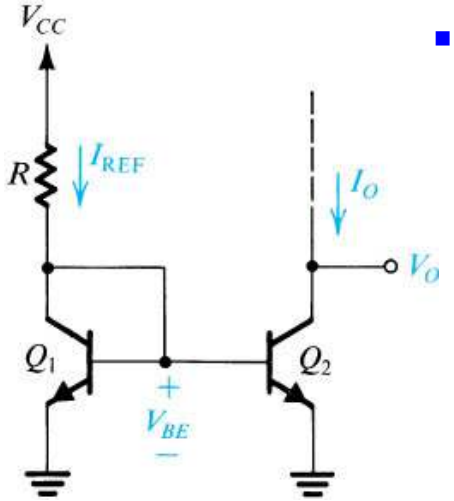
$$R_o \equiv \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O}$$

where V_{A2}& r_{o2} : Early voltage & output resistance

- *CTR* errors by the finite β & the finite R_o
- Error by Early effect = 0 for $V_O = V_{BE}$

$$I_O = I_{REF}\left(\frac{m}{1+\frac{m+1}{\beta}}\right)\left(1+\frac{V_O - V_{BE}}{V_{A2}}\right)$$

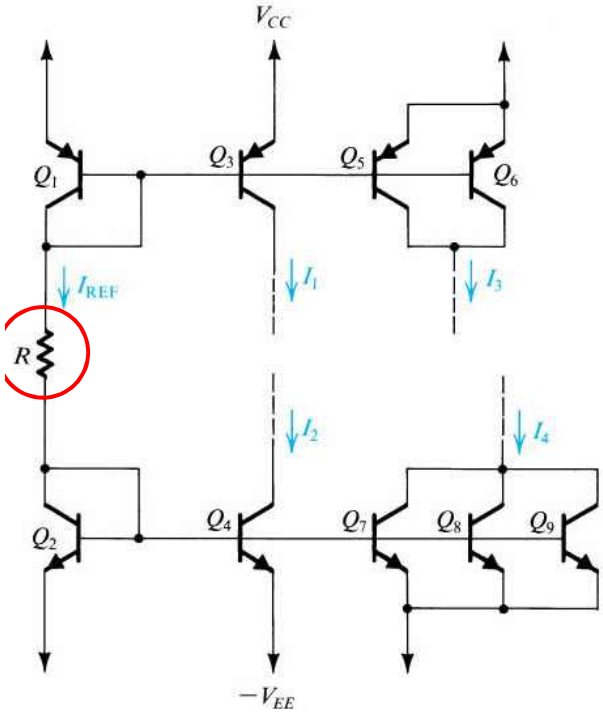
BJT Current-steering Circuits



- Simple Current Sink
  - reference current : $I_{REF} = \dfrac{V_{CC} - V_{BE}}{R}$ V_{BE} : corresponding to the desired I_{REF}

$$I_o = \frac{I_{REF}}{1 + (2/\beta)}\left(1 + \frac{V_O - V_{BE}}{V_A}\right)$$

  - Output resistance : $R_o = r_{o2} \cong \dfrac{V_A}{I_O} \cong \dfrac{V_A}{I_{REF}}$



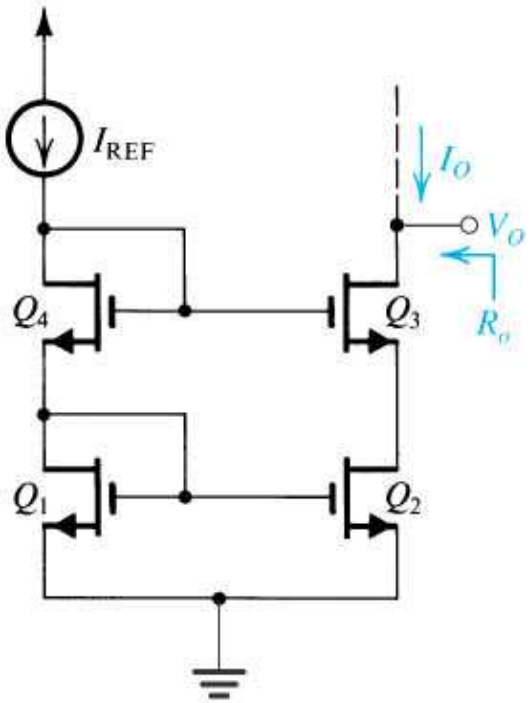
- Current Steering
  - generates bias currents for different amplifier stages in an IC
  - dc reference current I_{REF}

$$I_{REF} = \frac{V_{CC} + V_{EE} - V_{EB1} - V_{BE2}}{R}$$

  - sufficiently high β case, neglected I_B & neglected *Early effect*
    - * Q_3 : current mirror of Q_1 → $I_1 = I_{REF}$
      - active mode at Q_3 (*source*) : V_{C3} of $Q_3 < V_{CC}$-0.3V
    - * Q_5 & Q_6 in parallel → $I_3 = 2I_{REF}$
    - * Q_4 : mirror of Q_2 → $I_2 = I_{REF}$
      - active mode at Q_4 (*sink*) : V_{C4} of $Q_4 > -V_{EE}$+0.3V
    - * Q_7, Q_8 & Q_9 in parallel → $I_4 = 3I_{REF}$

Current-Mirror circuits w/ improved performance

- Constant-current source : biasing & active load
  - Performance parameters of current mirrors
    accuracy of the current transfer ratio of the mirror and output resistance of the current source
  - accuracy of the current transfer ratio suffers from the finite β of BJT
  - output resistance is limited to r_o of MOSFET & BJT
  → MOS & bipolar current mirrors with more accurate current transfer ratios and higher output resistances are required



- **Cascode MOS Mirrors**
  - diode-connected Q_1 → mirror $Q_1 - Q_2$
  - diode-connected Q_4 → bias voltage for gate of the cascode transistor Q_3
  - Output resistance R_o of cascode transistor Q_3

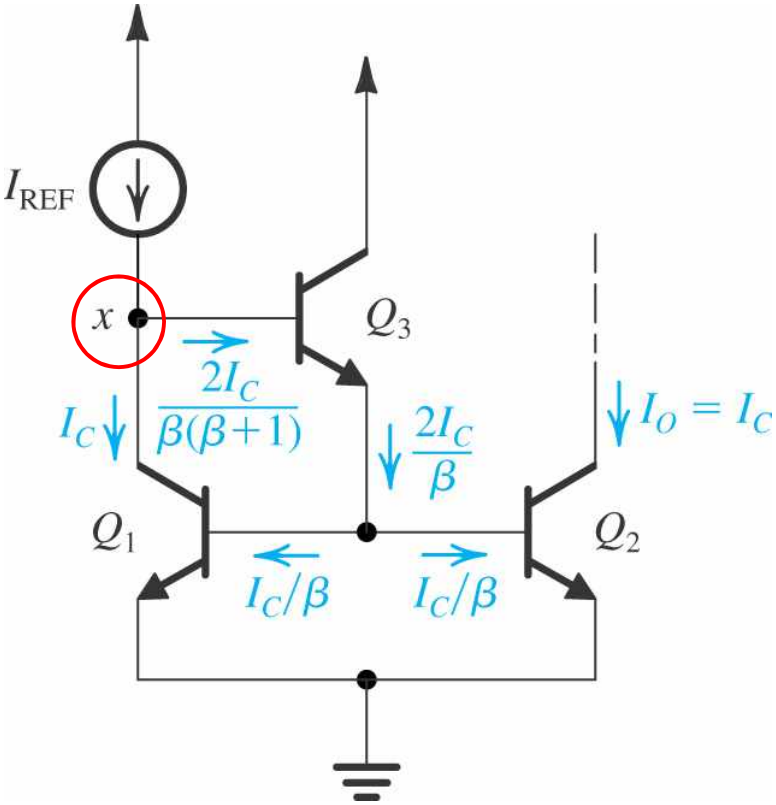
$$R_o \approx g_{m3} r_{o3} r_{o2}$$

  → cascoding raises R_o by the factor $(g_{m3}r_{o3})$, which is the intrinsic gain of the cascode transistor

  - Cascode current mirror consumes a relatively large portion of the steadily shrinking supply voltage V_{DD}.
  - Minimum voltage required across the output of the cascode mirror = $V_t + 2V_{OV}$ because gate of Q_3 is at $2V_{GS} = 2V_t + 2V_{OV}$ → 1V or so

A bipolar Mirror with Base-current Compensation

- Bipolar current mirror with a current transfer ratio that is much less dependent on β
  - Reduced dependence of β by including Q_3
  - Emitter of Q_3 supplies the base currents of Q_1 & Q_2
  - Sum of the base currents is divided by (β_3+1) → much smaller error current between I_{REF} & $I_C=I_O$



$$I_E = I_B + I_C = (1+\beta)I_B$$

- **Detailed analysis**
  - $Q_1 - Q_2$ are matched → equal collector currents, I_C
  - Node equation at the node labeled x :

$$I_{REF} = I_C\left[1+\frac{2}{\beta(\beta+1)}\right]$$

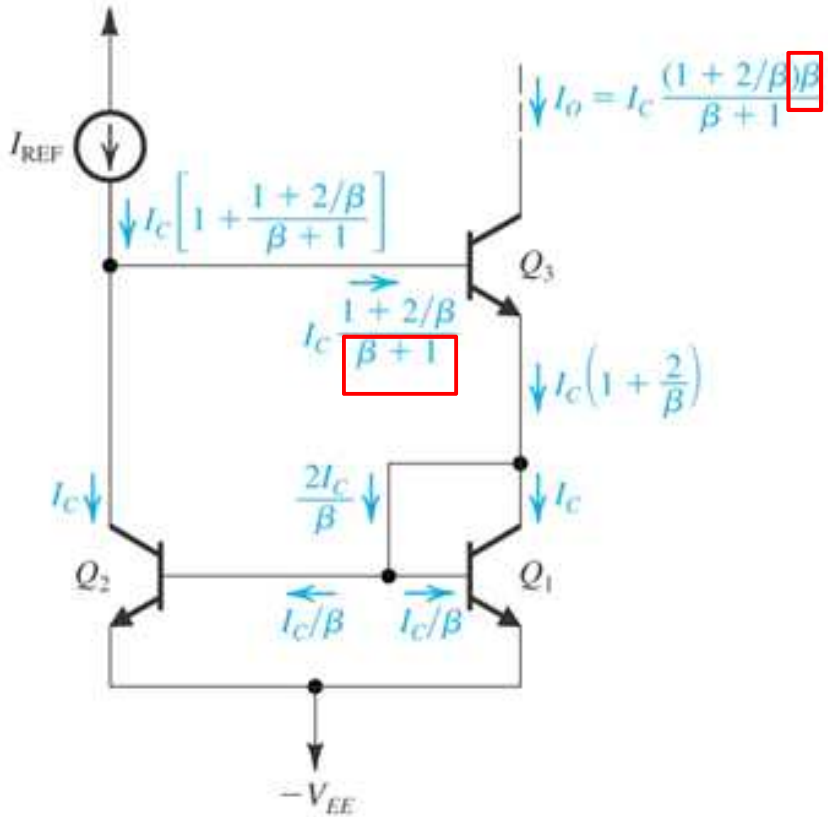
Since $I_O = I_C$

$$\frac{I_O}{I_{REF}} = \frac{1}{1+2/(\beta^2+\beta)} \approx \frac{1}{1+2/\beta^2}$$

  - error due to finite β : $2/\beta$ in the simple mirror → $2/\beta^2$
  - *output resistance* remains approximately *equal* to that of the simple mirror
  - When node x is connected to the power supply V_{CC} through a resistance R :

$$I_{REF} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R}$$

Wilson Current Mirror



$$I_E = I_B + I_C = (1+\beta)I_B \quad I_C = \beta I_B$$

▪ **Wilson Mirror** : both *reducing* the β dependence and *increasing* the output resistance

- Effect of finite β on the current transfer ratio :

assume Q_1 & Q_2 conduct equal collector currents

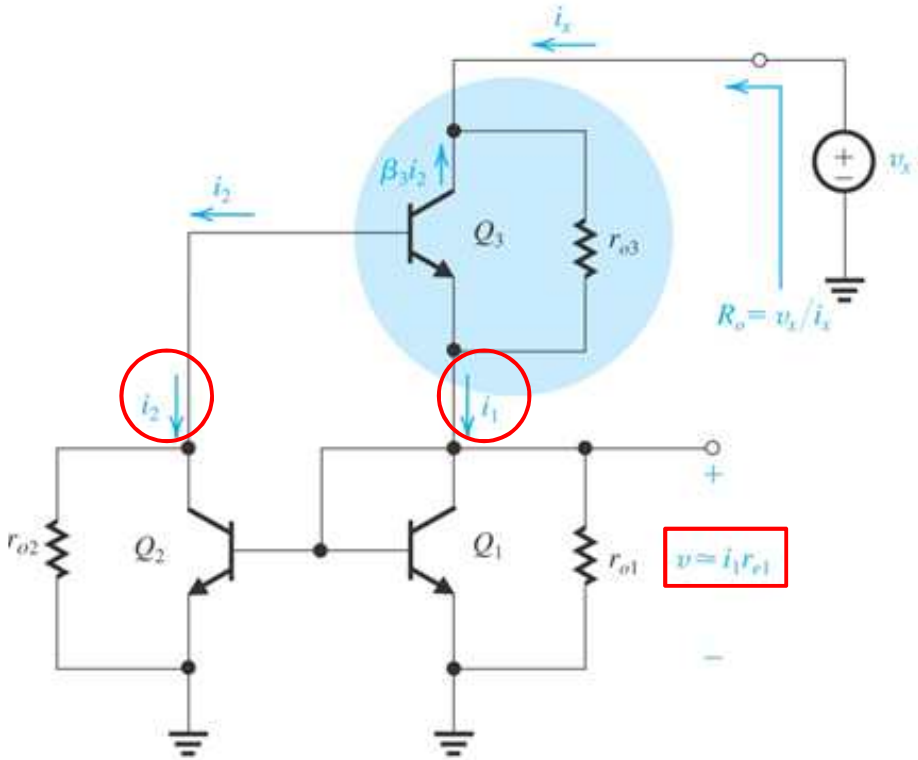
$$\frac{I_O}{I_{REF}} = \frac{I_C\left(1+\frac{2}{\beta}\right)\beta/(\beta+1)}{I_C\left[1+\left(1+\frac{2}{\beta}\right)\Big/(\beta+1)\right]} = \frac{\beta+2}{\beta+1+\frac{\beta+2}{\beta}} = \frac{\beta+2}{\beta+2+\frac{2}{\beta}}$$

$$= \frac{1}{1+\frac{2}{\beta(\beta+2)}} \approx \frac{1}{1+2/\beta^2}$$

- Collector-to-emitter voltage of Q_1 & Q_2 are not equal
  → a current offset or a systematic error
  → solved by adding a *diode-connected transistor* in series with the collector of Q_2 → MOS version

- Wilson mirror is *preferred* over the cascode circuit because the latter has the same dependence on β as the simple mirror

Wilson Current Mirror



▪ **Output resistance of Wilson mirror**

- set $I_{REF} = 0$ & apply a test voltage v_x to the output node

$$R_o = v_x / i_x$$

- direct analysis by "*pulled r_o out*" of each transistor

Q_3 as a supernode : $i_1 + i_2 = i_x$

by the action of current mirror Q_1- Q_2 : $i_2 \sim i_1 = i_x/2$

i_2 flows into the base of Q_3 → collector current $\beta_3 i_2$

current through r_{o3} → $i_x + \beta_3 i_2 = i_x + \beta_3(i_x/2) = i_x(\beta_3/2+1)$

voltage between the collector of Q_3 and ground = sum of the voltage drop across r_{o3} and the voltage v across Q_1

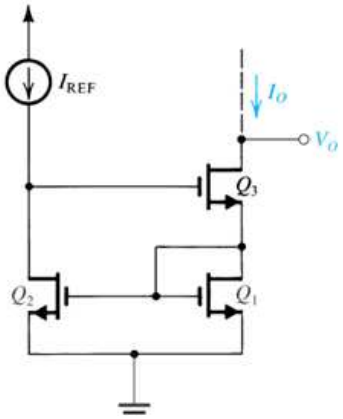
$$v_x = i_x\left(\frac{\beta_3}{2}+1\right)r_{o3} + i_1 r_{e1} = i_x\left(\frac{\beta_3}{2}+1\right)r_{o3} + \left(\frac{i_x}{2}\right)r_{e1}$$

Since $r_o >> r_e$ & $\beta_3 >> 2$,

$$v_x \approx i_x\left(\frac{\beta_3}{2}\right)r_{o3} \quad \triangleright \quad \boxed{R_o = \beta_3 r_{o3}/2}$$

- $\beta_3/2$ times higher output resistance than that of Q_3 alone = result of the *negative feedback* obtained by feeding the collector current of Q_2 (i_2) back to the base of Q_3
- The feedback *increases* the current through r_{o3} to approximately $\beta_3 i_x/2$, and thus the voltage across r_{o3} and the output resistance increase by the same factor, $\beta_3/2$.
- The factor ½ is because only half of i_x is mirrored back to the base of Q_3

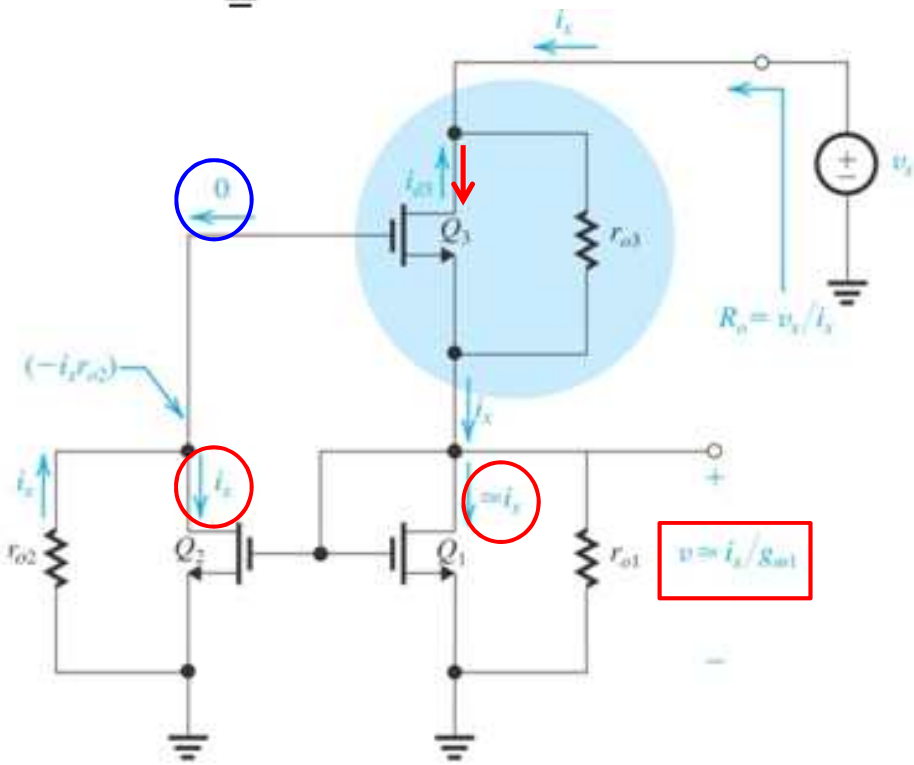
Wilson MOS Mirror



- MOS version of the Wilson mirror : enhanced output resistance
  but no β error to reduce like BJT version

- Output resistance : I_{REF}=0, and apply a test voltage v_x

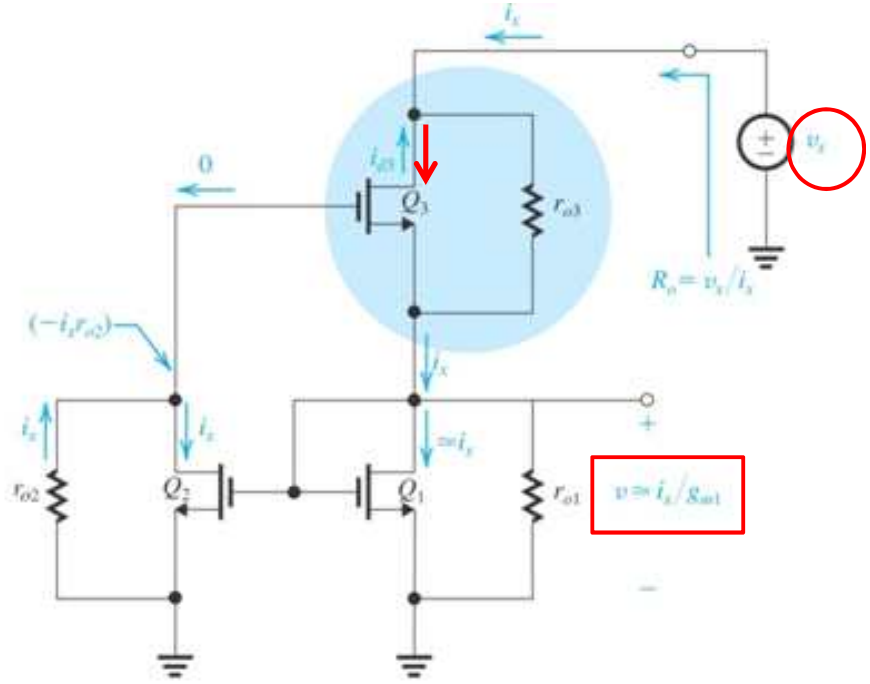
$$R_o = v_x / i_x$$

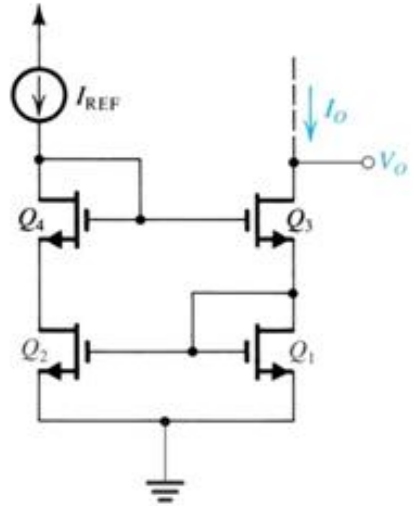


direct analysis by "*pulled r_o out*" of each transistor
input current of $Q_1 - Q_2$ mirror = i_x
Most of i_x flows in the drain proper of Q_1 → $v \sim i_x/g_{m1}$
Current-mirror action of (Q_1, Q_2) → i_x flows through the drain proper of Q_2
Since drain current of $Q_2 = 0$, all of i_x flows through r_{o2} → drain voltage of $Q_2 = -i_x r_{o2}$ → voltage fed back to the gate of Q_3
Drain current of Q_3 :

$$i_{d3} = g_{m3} v_{gs3} = g_{m3}\left(v_{g3} - v_{s3}\right)$$
$$= g_{m3}\left(-i_x r_{o2} - i_x / g_{m1}\right) \approx -\left(g_{m3} r_{o2}\right) i_x$$

Wilson MOS Mirror





A node eq. at the drain of Q_3 → current through r_{o3} :

$$(i_x - i_{d3}) = i_x + g_{m3}r_{o2}i_x \sim g_{m3}r_{o2}i_x$$

v_x = sum of the voltage drop across r_{o3} & voltage v across Q_1 :

$$v_x = g_{m3}r_{o2}i_x r_{o3} + v = (g_{m3}r_{o3}r_{o2})i_x + (i_x/g_{m1})$$

$$\approx g_{m3}r_{o3}r_{o2}i_x$$

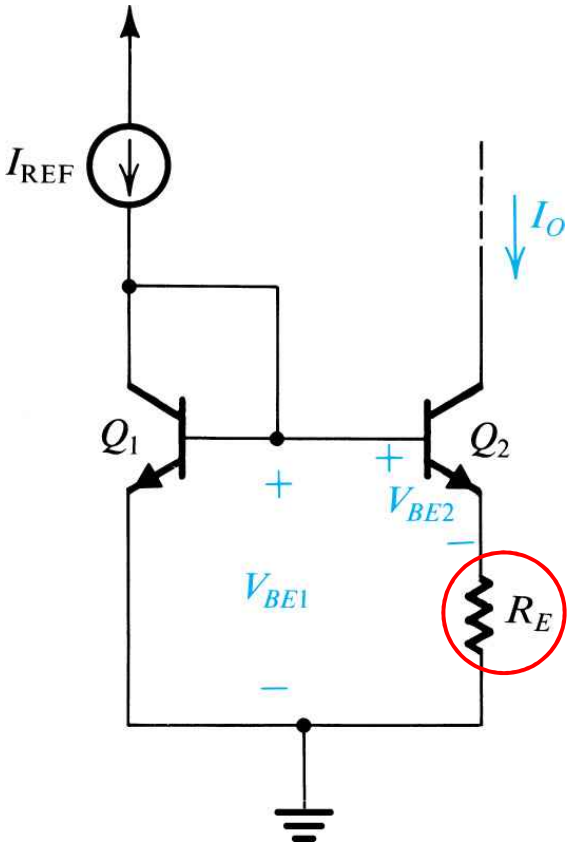
$$R_o = \frac{v_x}{i_x} = (g_{m3}r_{o3})r_{o2}$$

Wilson MOS mirror : increase of output resistance by a factor of $(g_{m3}r_{o3})$ = identical result in the cascode mirror

Increase in R_o → a negative feedback result obtained by connecting the drain of Q_2 to the gate of Q_3

(c) modified circuit to balance the two branches of the mirror and thus avoid the systematic current error resulting from the difference in V_{DS} between Q_1 and Q_2

Widlar Current Source



A resistor R_E is included in the emitter lead of Q_2.
Neglecting base currents, and Q_1 & Q_2 are matched :

$$V_{BE1} = V_T \ln\left(\frac{I_{REF}}{I_S}\right), \quad V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right)$$

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$$

From the circuit :

$$V_{BE1} = V_{BE2} + I_O R_E$$

$$\triangleright \quad I_O R_E = V_T \ln\left(\frac{I_{REF}}{I_O}\right)$$

- Widlar circuit allows the generation of a *small constant current* using relatively *small resistors*. → considerable savings in chip area.
- High output resistance due to the *emitter-degeneration resistance* R_E

$$R_{out} \approx \left[1 + g_m\left(R_E \,\|\, r_\pi\right)\right] r_o$$