Microelectronic Circuits I

Ch 5
MOS Field-Effect Transistors (MOSFETs)

5.1 Device Structure and Physical Operation
5.2 Current – Voltage Characteristics

MOSFET *vs.* Diode

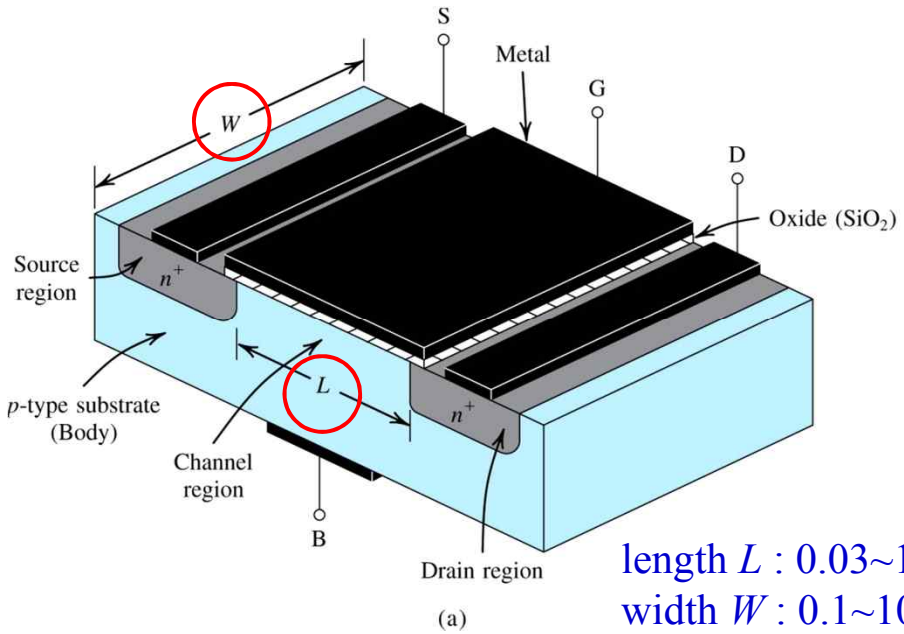
	MOSFET	Diode
Terminal	Three terminal device: *use of the voltage between 2 terminals to control the current in the 3rd terminal* → controlled source, switch	Two terminal : Uncontrolled switch
Merits	•Smaller size •Simple manufacturing process •Little power → VLSI (2 billion)	
Applications	•Amplification •Microprocessor, Memory chips •Digital logic, Analog ICs • mixed-signal chip	•Rectifier

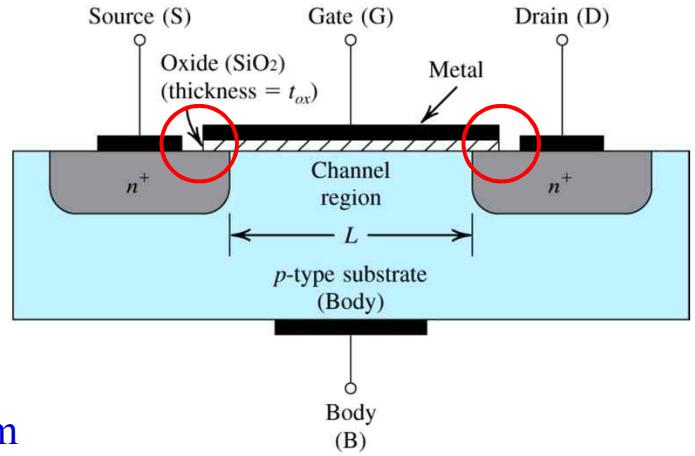
*MOSFET: **M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor

→ *the most widely used electronic devices*

Device structure and Physical Operation

n-channel *enhancement*-type MOSFET





length L : 0.03~1μm
width W : 0.1~100μm

- *p*-type substrate : physical support for the devices → body
- heavily doped *n*-type n^+ silicon : n^+ source & n^+ drain
- thin layer of silicon dioxide (SiO_2 : t_{ox}= 1~10 nm) : electrical insulator → insulated-gate FET
- Metal deposited on top of the oxide layer : gate electrode → Metal-Oxide-Semiconductor FET
- 4 terminals : gate (G), source (S), drain (D) and substrate or body (B)
  → connecting B to S : 3 terminals [G, S, D]
- symmetrical device : a voltage at Gate controls current flow between Drain and Source

Operation of MOSFET

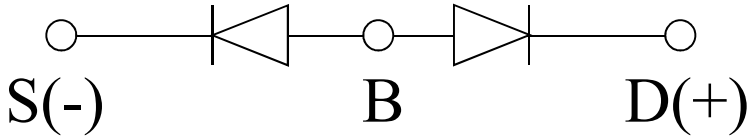
- Operation with No Gate Voltage

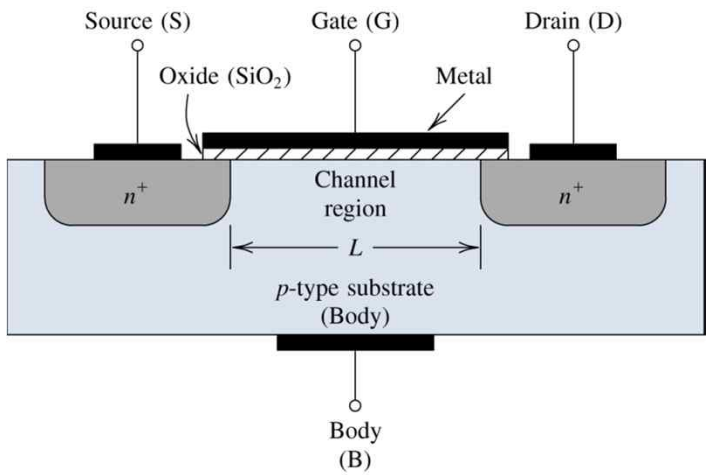
  When $v_{GS} = 0$, $v_{DS} > 0$

  – *Body* is connected to *source*. (3-terminal)

  – Two *pn* junctions (*substrate-drain* & *substrate-source*) are cut-off. ($I = 0$)

  – Path between *D* & *S* : very high resistance (of the order of 10^{12} Ω)

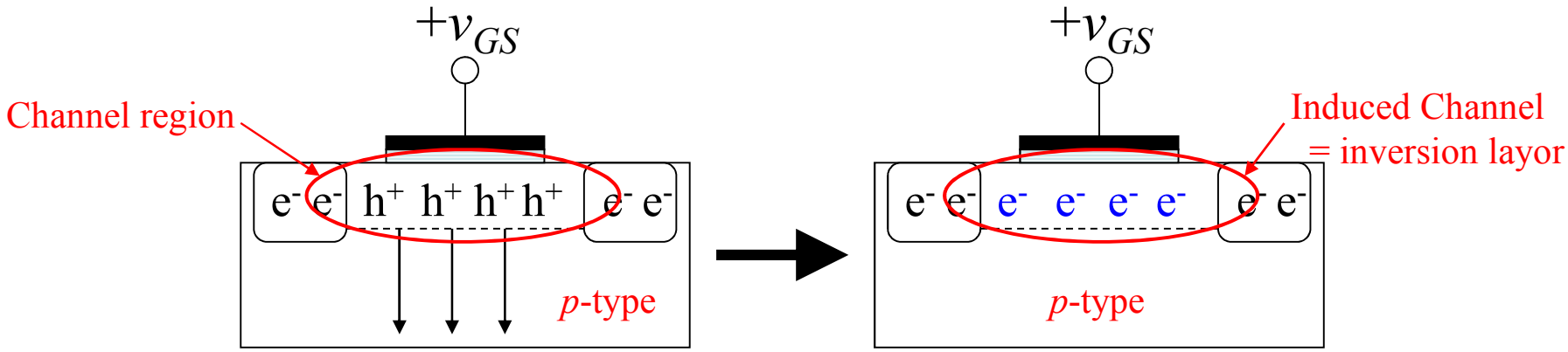




Two back-to-back diodes prevent current conduction from drain to source when v_{DS} is applied

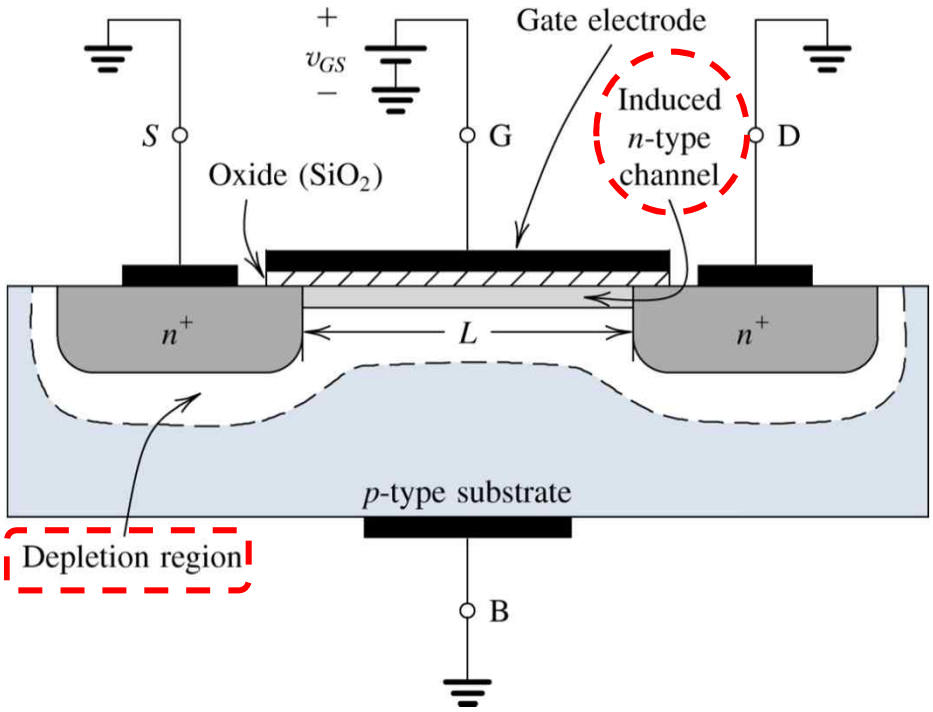
Creating a Channel for Current Flow

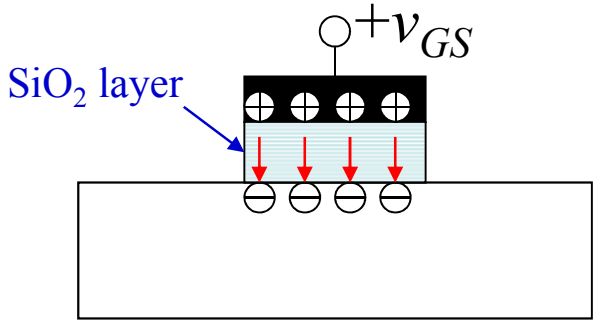
- When $v_{GS} > 0$, $v_{DS} = 0$ (Source, Drain & Body are grounded)



- *Mechanism for Channel induction:*
  - $v_{GS} > 0$ → Holes at the channel region are pushed downward into the substrate.
  - A carrier depletion region at the channel region →uncovered negative charges
  - v_{GS} attracts electrons from n^+ source & n^+ drain into the channel region.
    → *n* region connecting *S* and *D* is in effect created
    → if $v_{DS} > 0$, current flows through this induces *n* region
  - The induced *n* region forms a channel for current flow from drain to source
    → *n-channel MOSFET or NMOS transistor*
  - Channel : inverts the substrate surface from *p* type to *n* type → **inversion layer**

Creating a Channel for Current Flow

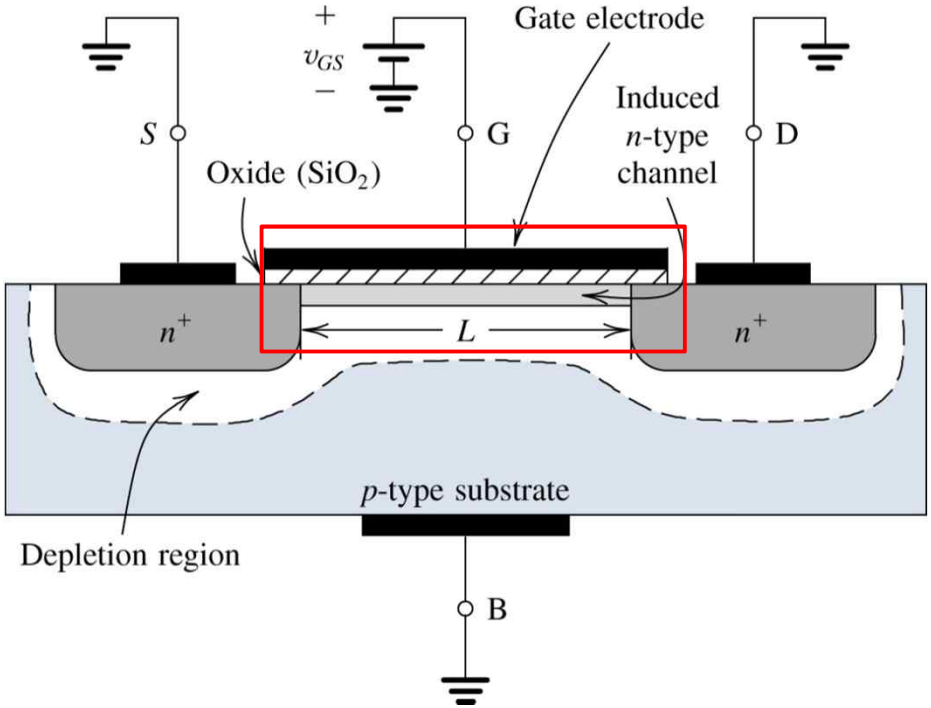




*Parallel-plate capacitor

- *Threshold voltage* V_t (0.3 ~ 1 V) **:**
  v_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel.
- *Parallel plate capacitor* :
  - oxide layer : dielectric, gate : positive plate, induced channel : negative plate
  - Electric field → controls the amount of charge in the channel →channel conductivity
    → current flowing through the channel when v_{DS} is applied
    → field-effect transistor (FET)

Creating a Channel for Current Flow



- The voltage across the parallel-plate capacitor must exceed V_t for a channel to form
- When $v_{DS} = 0$, voltage across the oxide is uniform & equal to v_{GS}
- **Overdrive voltage** or **effective voltage** : excess of v_{GS} over V_t

$$v_{GS} - V_t \equiv v_{OV}$$

- Electron charge in the channel

$$|Q| = C_{ox}(WL)v_{OV}$$

- **Oxide capacitance C_{ox}** : capacitance of the parallel-plate capacitor per unit gate area (F/m^2)

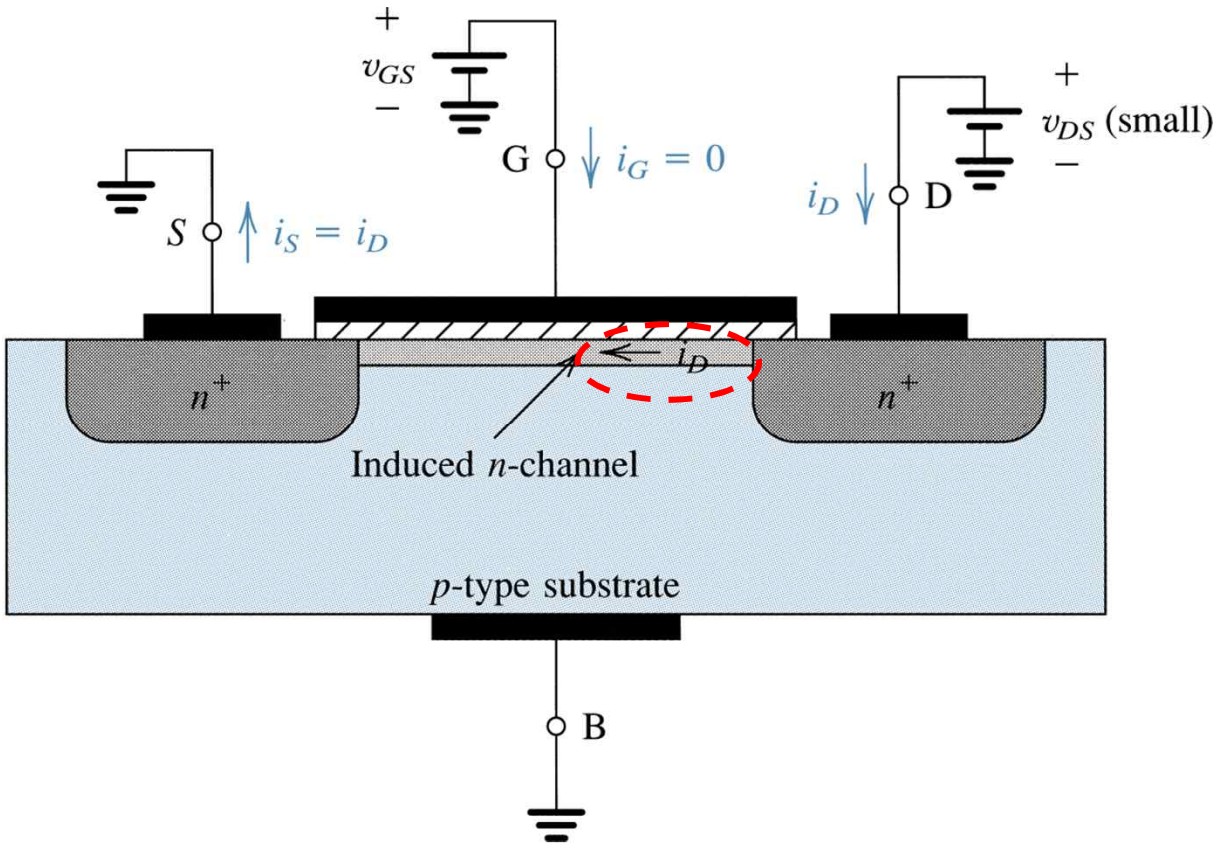
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$\varepsilon_{ox}=3.9\varepsilon_0=3.9\text{x}8.954\text{x}10^{-12}=3.24\text{x}10^{-11}$ F/m : *permittivity* of SiO_2
$C_{ox}=8.6\text{x}10^{-3}$ F/m^2 @ $t_{ox}=4$nm
$C=C_{ox}WL=1.1f$F @ $L=0.18\mu$m, $W=0.72\mu$m, fP : femptofarad(10^{-15} F)

- as v_{GS} increases, the magnitude of channel charge increases proportionately
  → increase in the depth of the channel
- The larger the overdrive voltage v_{OV}, the deeper the channel

Applying a Small v_{DS}

- When a small positive v_{DS} is applied. ($v_{DS} \sim 50\text{mV}$)

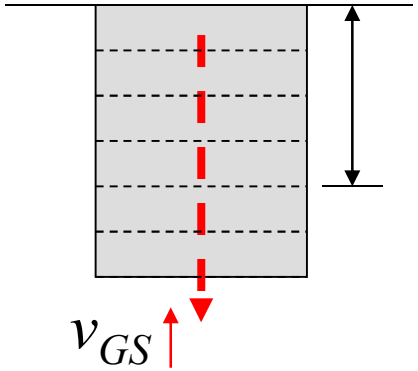


The voltage v_{DS} causes a current i_D to flow through the induced n channel

Applying a Small v_{DS}

- i_D current flow:
  - Current is carried by free electrons traveling from *source* to *drain*
    → the reason for *source* and *drain*
  - The direction of current i_D flow : from *drain* to *source*
  - The magnitude of i_D depends the *density of electrons* in the channel
    → depends on the magnitude of v_{GS}

- excess gate voltage **(= v_{GS} - V_t),** Effective voltage or overdrive voltage **:**
  - As v_{GS} exceeds V_t , more electrons attracted into the channel
    : *the increase in charge carriers in the channel*
    → increase in the channel depth, increased channel conductance, reduced channel resistance



Channel depth ↑ ⟶ Channel conductance ↑

$$i_S = i_D, i_G = 0$$
$$i_D \propto (v_{GS} - V_t) \;\&\; v_{DS}$$

Applying a Small v_{DS}

- i_D calculation

  - small v_{DS} → voltage between G & channel is remains constant & equal to v_{GS}
    → effective voltage between G & channel = v_{OV}

  - charge per unit channel length : $$\frac{|Q|}{unit\ \ channel\ \ length} = C_{ox} W v_{OV}$$

  - Electric field E across the length of the channel by v_{DS} : $$|E| = \frac{v_{DS}}{L}$$

    Electron drift velocity $= \mu_n |E| = \mu_n (v_{DS}/L)$ μ_n : electron mobility

  - i_D by multiplying the charge per unit channel length by electron drift velocity

$$i_D = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) v_{OV} \right] v_{DS} = \left[(\mu_n C_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t) \right] v_{DS}$$

  - Conductance g_{DS} of the channel

$$g_{DS} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) v_{OV} = (\mu_n C_{ox}) \left(\frac{W}{L} \right) (v_{GS} - V_t)$$

  - Conductance g_{DS} : product of $(\mu_n C_{ox})$, (W/L), v_{OV} $(= v_{GS}\text{-}V_t)$

Applying a Small v_{DS}

- Conductance g_{DS} : product of $(\mu_n C_{ox})$, (W/L), v_{OV} $(= v_{GS}\text{-}V_t)$
  - $k_n' = \mu_n C_{ox}$: process transconductance parameter [A/V^2]
  - aspect ratio (W/L) : minimum channel length (2009) ~ 45 nm, t_{ox} ~ 1.4nm
  - MOSFET transconductance parameter k_n [A/V^2]:

$$k_n = k_n'(W/L) = (\mu_n C_{ox})(W/L)$$

  - overdrive voltage $v_{OV} = v_{GS}\text{-}V_t$

- With v_{DS} kept small, MOSFET behaves as a linear resistance r_{DS} controlled by v_{GS}

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{(\mu_n C_{ox})(W/L)v_{OV}} = \frac{1}{(\mu_n C_{ox})(W/L)(v_{GS} - V_t)}$$

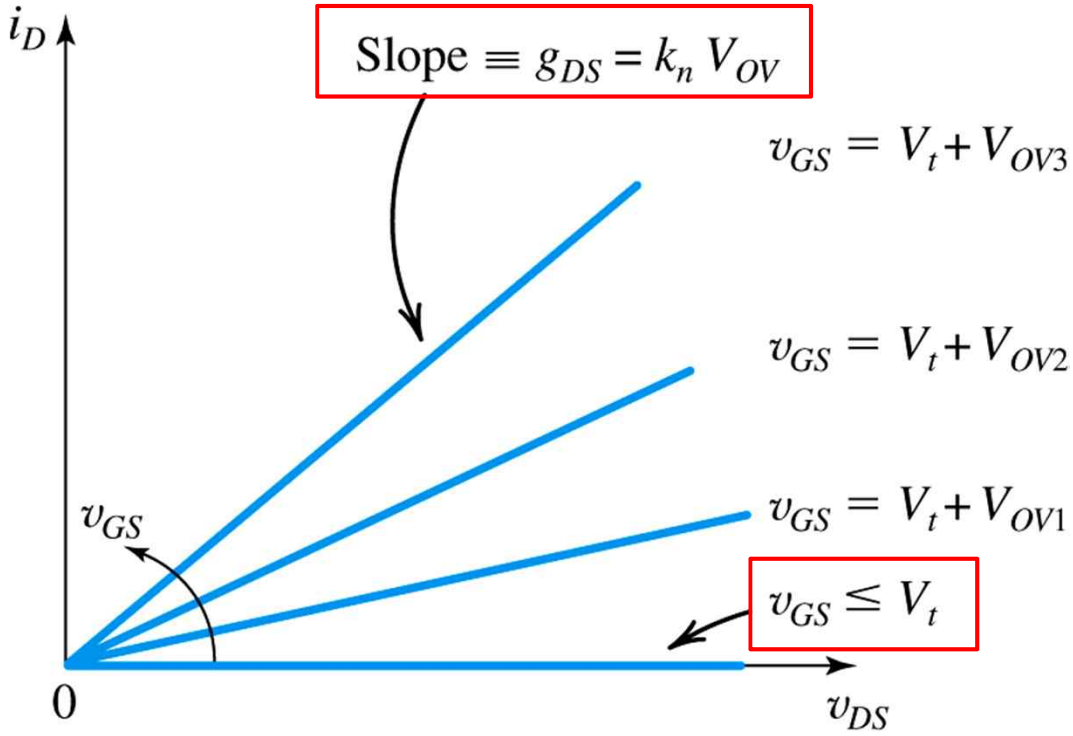
- i_D when v_{DS} is small (~ 50mV)

$$i_D = k_n'\left(\frac{W}{L}\right)\boxed{v_{OV}}v_{DS}$$

Applying a Small v_{DS}

- MOSFET device is operating as a linear resistance whose value is controlled by v_{GS} when v_{DS} is kept small

- The resistance is infinite for $v_{GS} < V_t$, and its value decreases as v_{GS} exceeds V_t
- The graph depends only on v_{OV}
- For the MOSFET to conduct, a channel has to be induced
- $i_S = i_D$, and $i_G = 0$



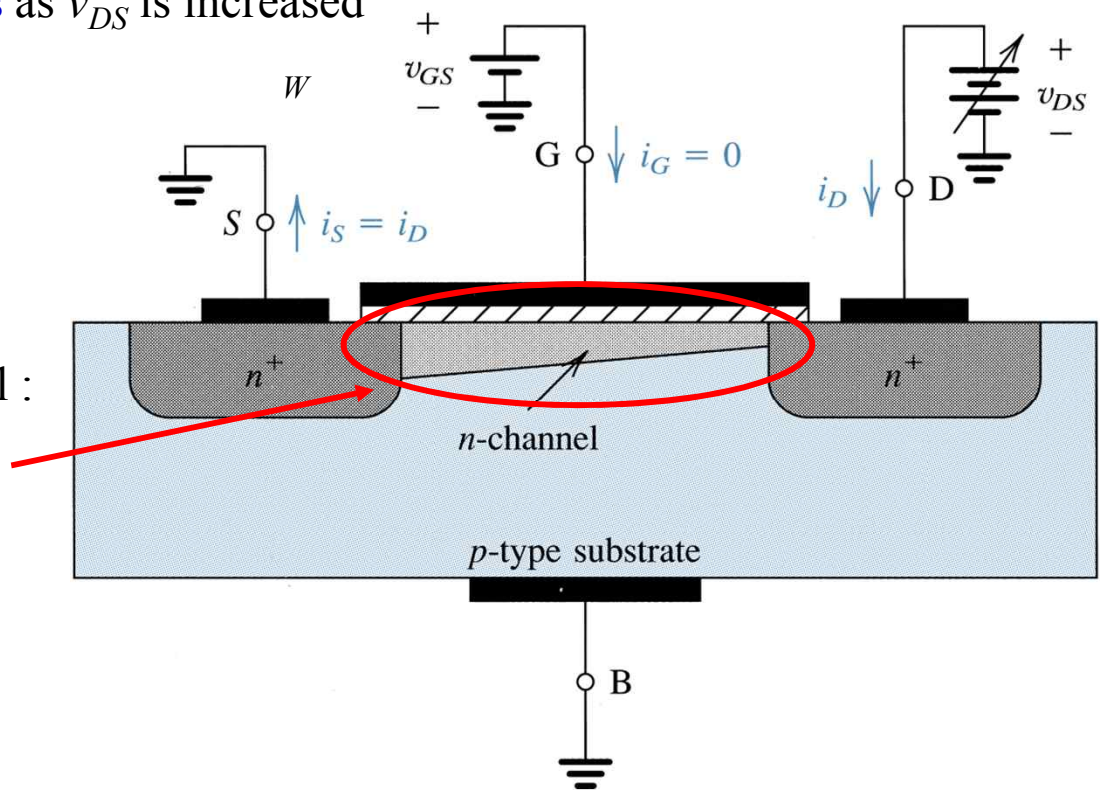
- Enhancement-mode operation (enhancement-type MOSFET): increasing v_{GS} above the threshold voltage V_t enhances the channel.

Operation as v_{DS} is Increased

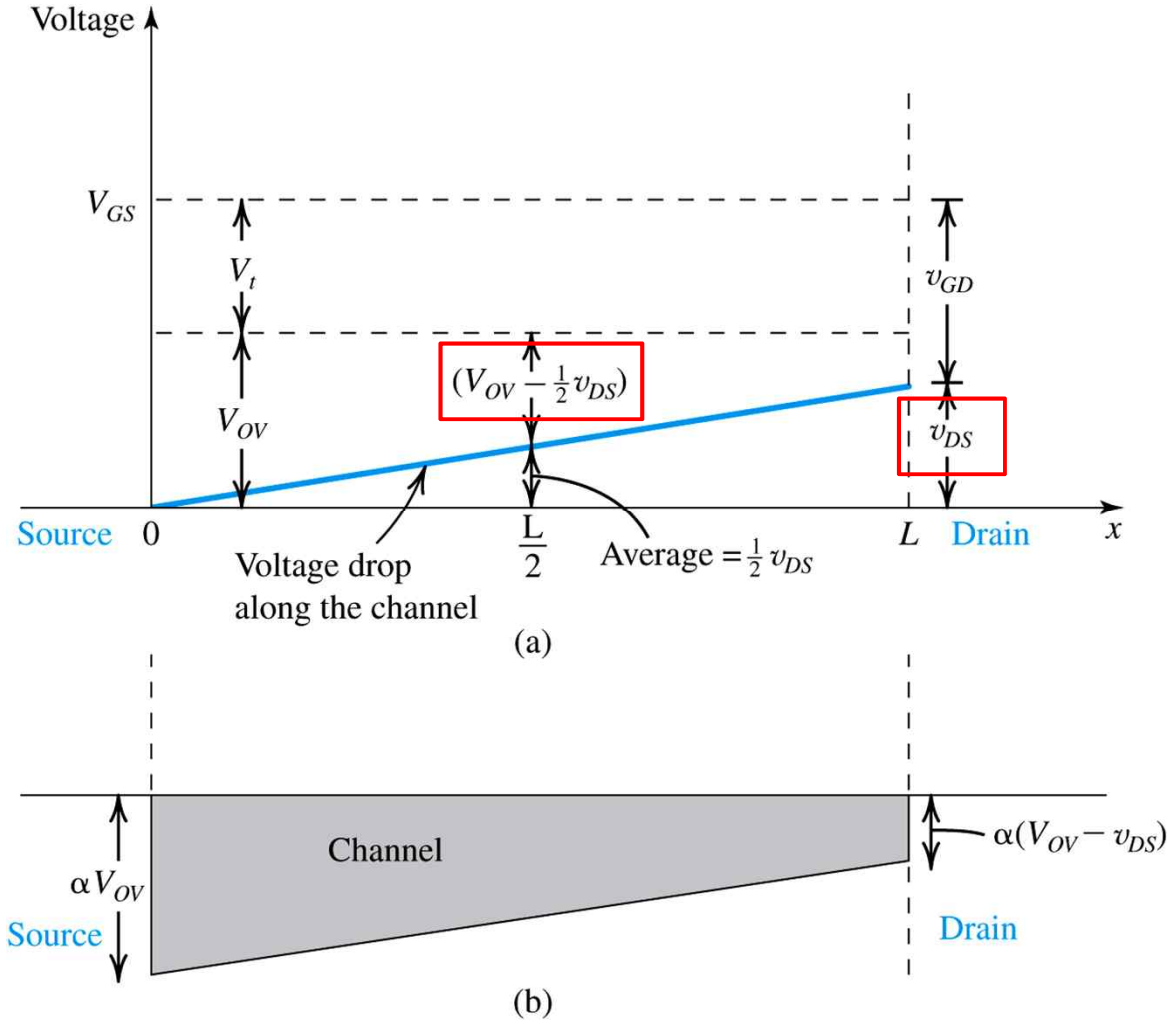
When v_{DS} increases with $v_{GS} > V_t$ & kept constant.

- v_{DS} appears as a voltage drop across the length of channel
- the voltage increases from 0 to v_{DS} along the channel from *Source* to *Drain*
- the voltage between the *Gate* and points along the channel decreases from $v_{GS} = V_t + V_{OV}$ at S to $v_{GD} = v_{GS} - v_{DS} = V_t + V_{OV} - v_{DS}$ at D
- channel depth $\propto$ the above voltage difference
  - → The induced channel has a tapered shape, deepest at S & shallowest at D
  - → its resistance increases as v_{DS} is increased

Tapered form of induced channel :
deepest at the source end &
shallowest at the drain end



Operation as v_{DS} is Increased



Charge in the tapered channel

$\propto$ channel cross-sectional area

$\propto \frac{1}{2}\left[V_{OV} + \left(V_{OV} - v_{DS}\right)\right]$

or $\left(V_{OV} - \frac{1}{2}v_{DS}\right)$

by replacing V_{OV} by $(V_{OV}\text{-}1/2v_{DS})$

$$i_D = k_n'\left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

$$= k_n'\left(\frac{W}{L}\right)\left(V_{OV}v_{DS} - \frac{1}{2}v_{DS}^2\right)$$

$$= k_n'\left(\frac{W}{L}\right)\left((v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right)$$

$i_D - v_{DS}$ characteristic
in the triode region

Figure 5.6(a) For a MOSFET with $v_{GS} = V_t + V_{OV}$, application of v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $\frac{1}{2}v_{DS}$ at the midpoint. Since $v_{GD} > V_t$, the channel still exists at the drain end. **(b)** The channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to V_{OV}, that at the drain end is proporational to $(V_{OV} - v_{DS})$.

Operation as v_{DS} is Increased

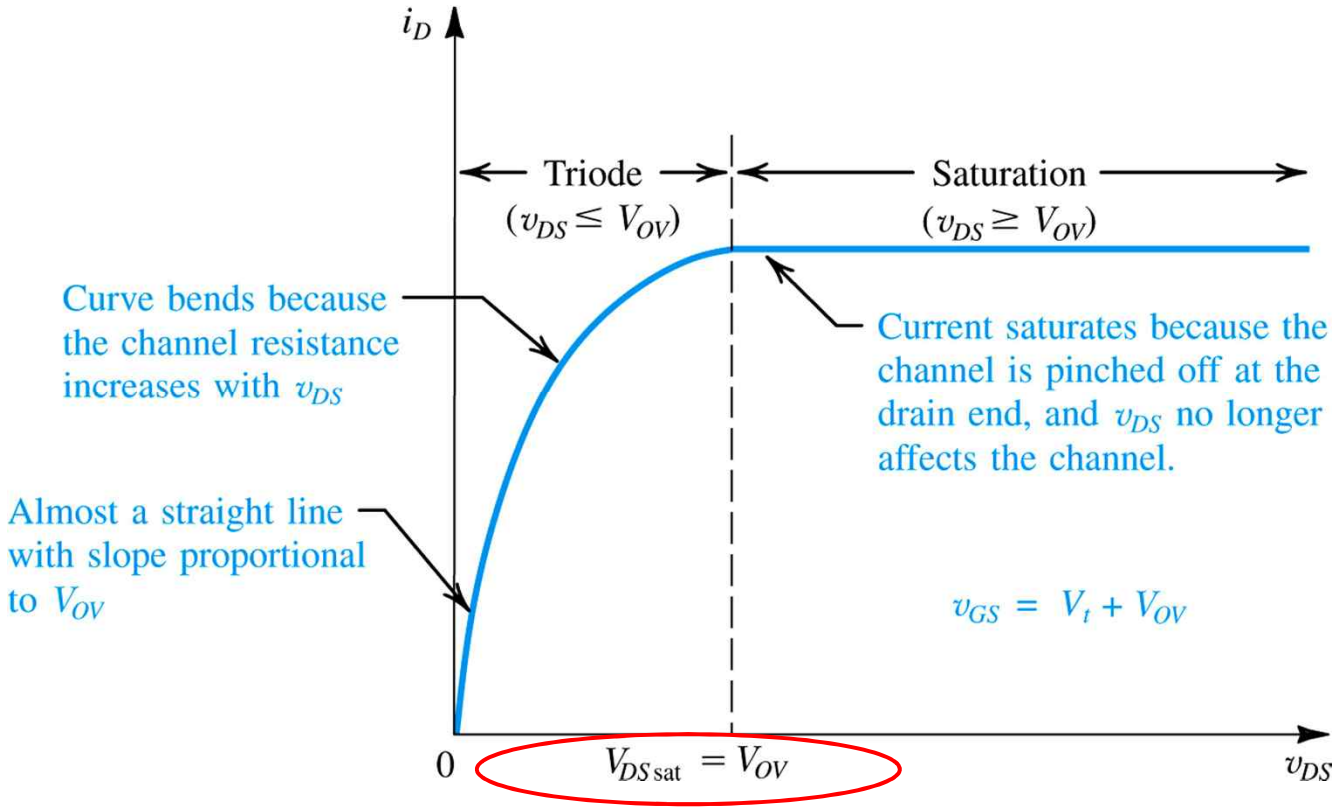
As v_{DS} is increased, the channel becomes more tapered and its resistance increases

i_D - v_{DS} curve does not continuous as a straight line but bends, as v_{DS} is increased

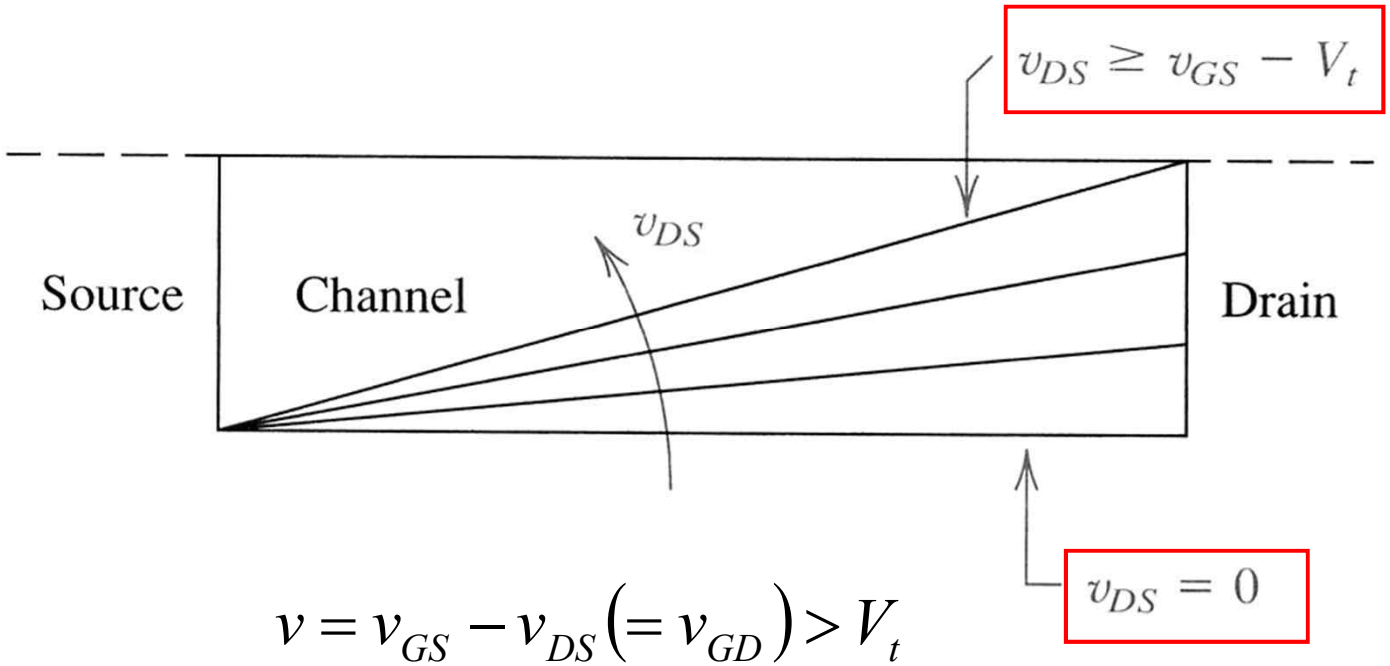
→ *semiparabolic* portion of i_D - v_{DS} curve

As v_{DS} is reduced, we can neglect $1/2 v_{DS}$ relative to V_{OV}

$$i_D = k_n'\left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}v_{DS}\right)v_{DS} \quad \triangleright \quad i_D = k_n'\left(\frac{W}{L}\right)V_{OV}v_{DS} \qquad @ \text{ small } v_{DS}$$



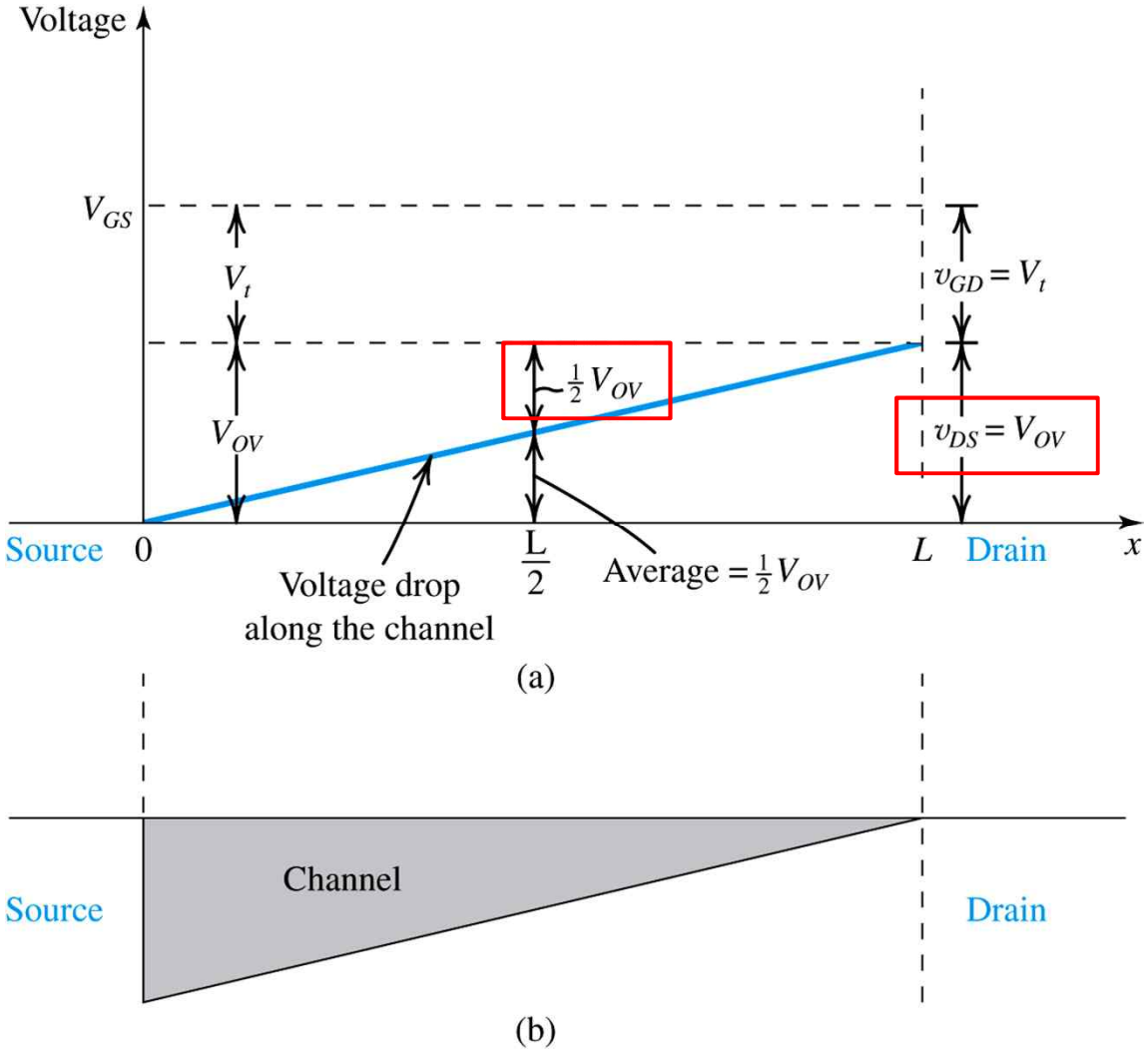
Operation for $v_{DS} >> V_{OV}$



$$v = v_{GS} - v_{DS}\left(= v_{GD}\right) > V_t$$
$$\rightarrow v_{DS} < \left(v_{GS} - V_t\right)$$

- Increasing v_{DS} causes the channel to acquire a tapered shape
- As v_{DS} reaches V_{OV} ($=v_{GS} - V_t$), the channel is pinched off at the drain end
  Pinch-off : the disappearance of the conducting channel adjacent to the drain
- Increasing v_{DS} above $v_{GS} - V_t$ ($= V_{OV}$) has little effect on the channel's shape & charge
  → current through the channel remains constant at the value @ $v_{DS}=V_{OV}$
  → The current thus **saturates**

Operation for $v_{DS} >> V_{OV}$



- Channel pinch-off does *not* mean channel blockage
- Any increase in v_{DS} above V_{DSsat} $(=V_{OV})$ appears as a voltage drop across the depletion region
- Both the current through the channel and the voltage drop across it r*emains* constant in saturation

Figure 5.8 Operation of MOSFET with $v_{GS} = V_t + V_{OV}$, as v_{DS} is increased to V_{OV}. At the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $V_{DSat} = V_{OV}$) has no effect on the channel shape and i_D remains constant.

Operation for $v_{DS} >> V_{OV}$

Current through the channel saturates at the value for $v_{DS}=V_{OV}$ → **saturation region**

$$i_D = k_n'\left(\frac{W}{L}\right)\frac{1}{2}V_{OV}V_{DSsat} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS}-V_t)^2$$

$$V_{DSsat} = V_{OV} = V_{GS} - V_t$$

→ In saturation region, i_D remains constant for a given v_{GS} as v_{DS} is varied
→ $i_D - v_{DS}$ curve is a horizontal straight line as shown in ppt 15

- $i_D - v_{DS}$ relationship

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS}-V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

triode region
(continuous channel)

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS}-V_t)^2 = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

saturation region
(pinch-off channel)

The *p*-Channel MOSFET (PMOS)

- *p*-channel enhancement-type MOSFET (PMOS transistor)
  - *n*-type substrate
  - p^+ region : drain & source → charge carrier is *hole*
  - v_{GS}, v_{DS} & $V_t < 0$
  - induced *p*-channel

$$v_{GS} \le V_{tp} \qquad |v_{GS}| \ge |V_{tp}|$$

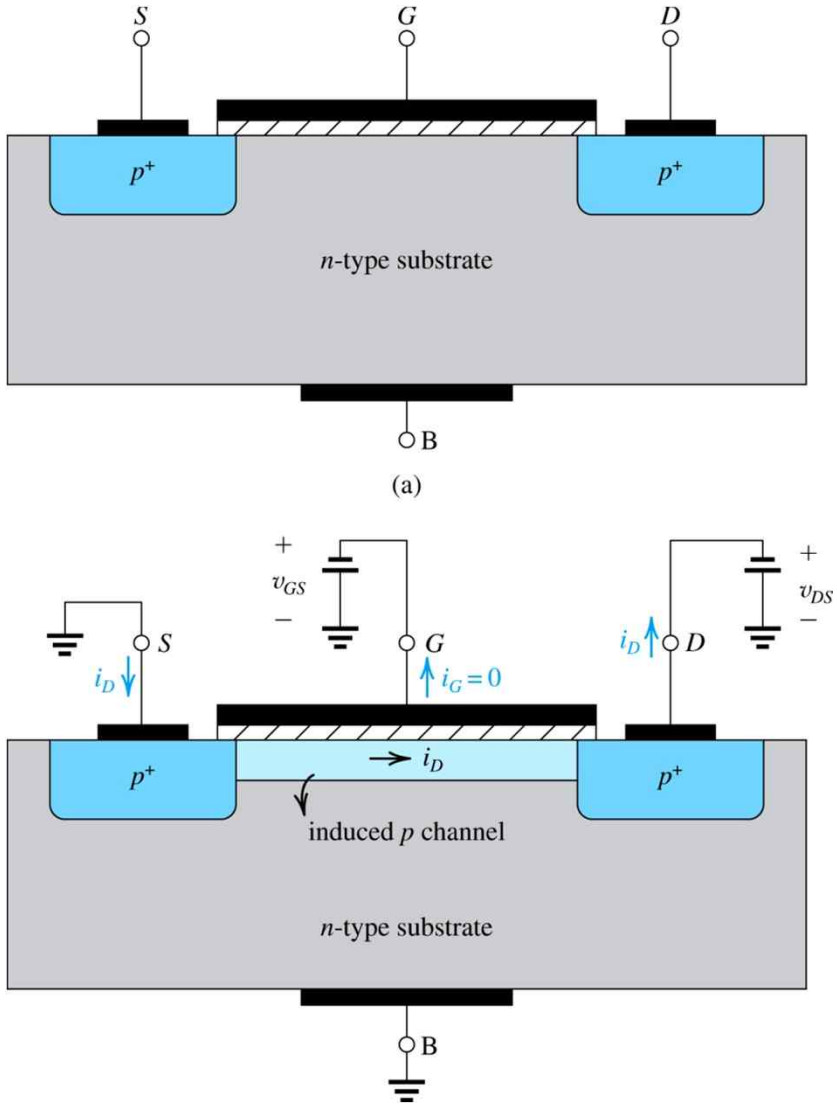
  - i_D flows through the channel from the *source* to *drain* by a negative v_{DS}
  - Process transconductance parameter

$$k_p' = \mu_p C_{ox} \qquad \mu_p = 0.25 \sim 0.5\mu_n$$

  - Transistor transconductance parameter

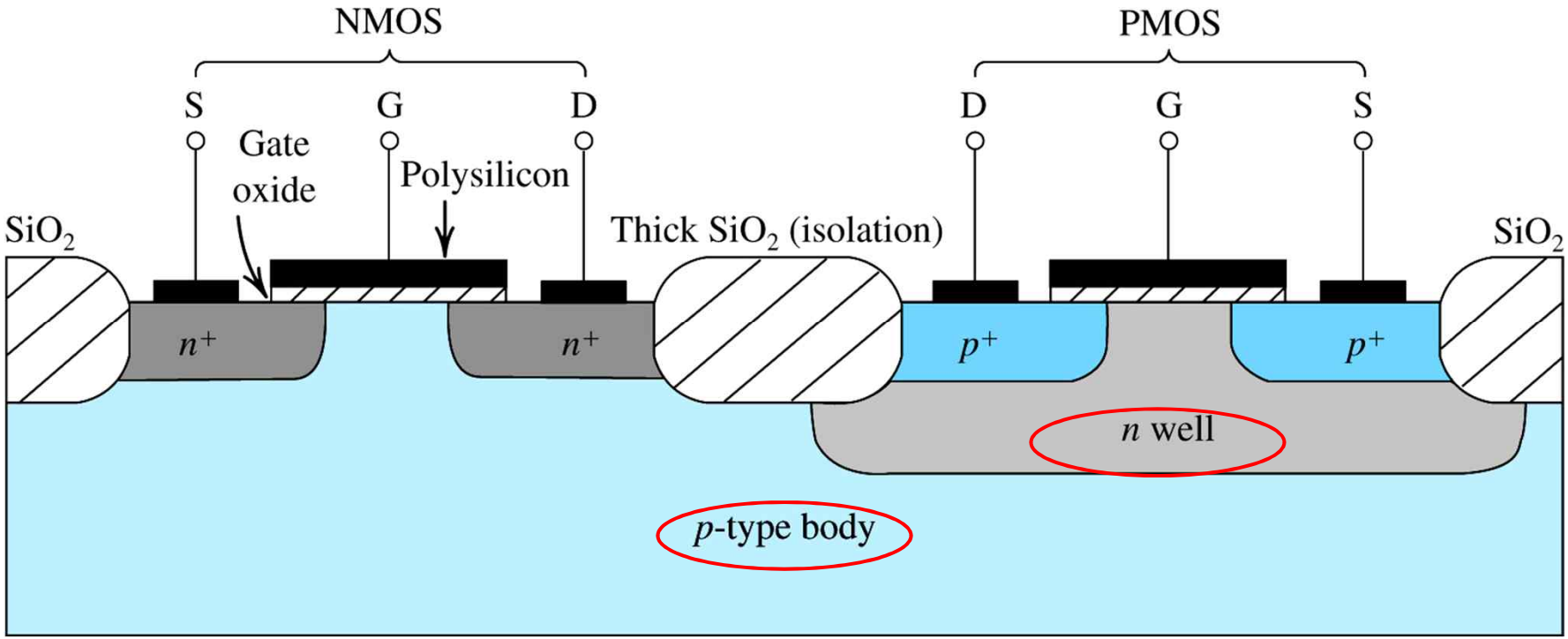
$$k_p = k_p'(W/L)$$

  - Electron mobility μ_n is higher than a factor of 2 to 4 than hole mobility μ_p
    → NMOS speed > PMOS speed



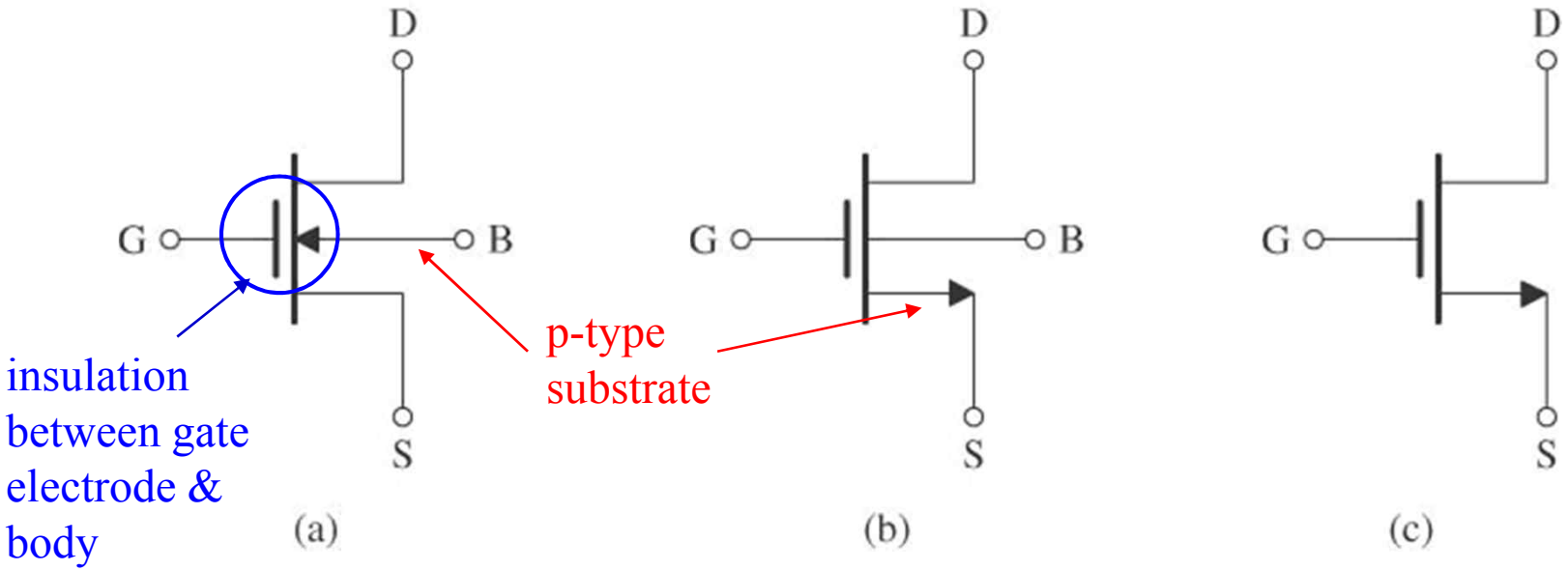
Complementary MOS or CMOS

- CMOS: NMOS + PMOS
- The most widely used of all the IC technologies
- PMOS is formed in a separated *n*-type region, known as an ***n well***
- NMOS & PMOS are isolated by a thick region of *oxide* that function as an insulator



Current – Voltage Characteristics

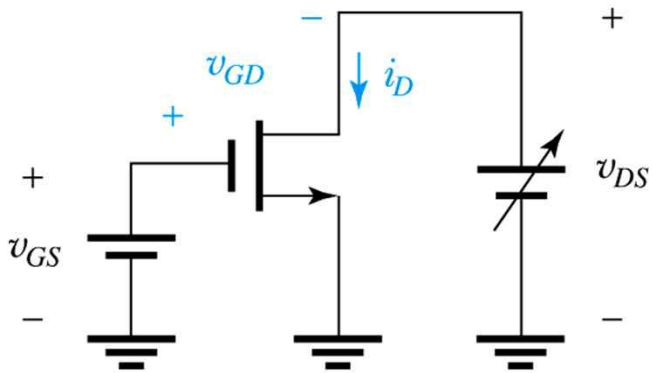
Circuit symbol of *n*-channel enhancement-type MOSFET

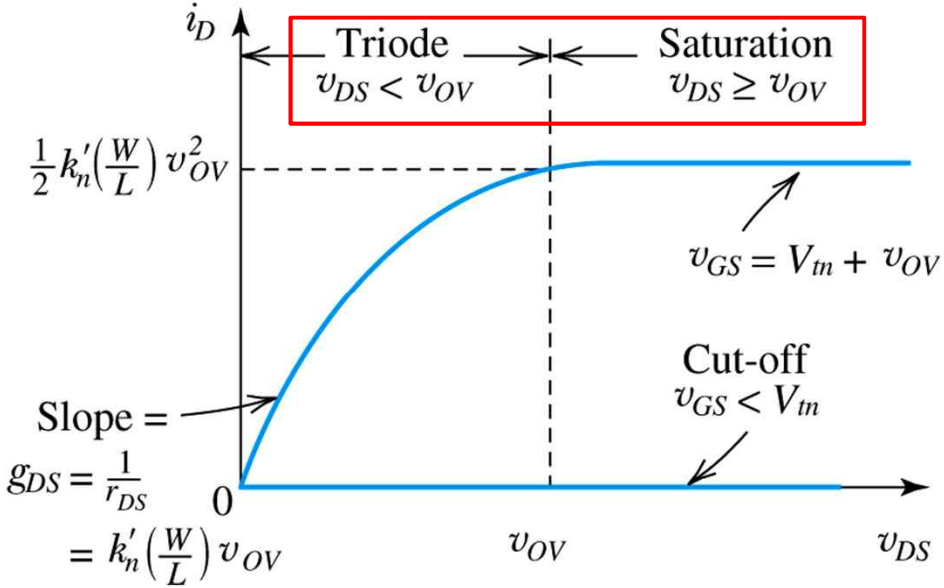


(a) Circuit symbol for the *n*-channel enhancement-type MOSFET. **(b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel). **(c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

- *The drain is always positive relative to the source in an n-channel FET*
- *arrowhead : normal direction of current flow*

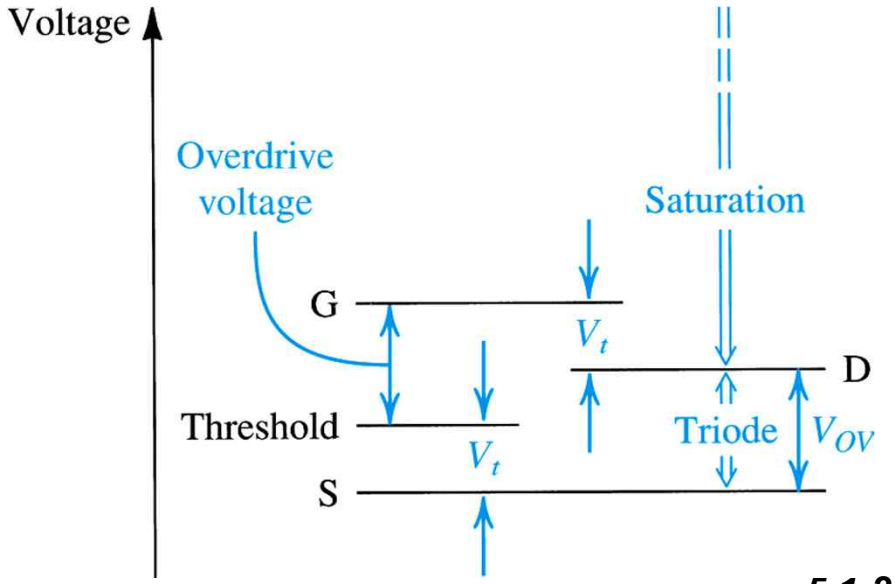
$i_D - v_{DS}$ Characteristics





- Cutoff region → switch (off)
- Triode region → switch (on)
- Saturation region → amplifier

- Boundary between triode and saturation : whether v_{DS} is less or greater than v_{OV}
- Triode region : v_G must exceed v_D by more than V_{tn} → continuous channel
- Saturation region : $v_D > v_G - V_{tn}$, v_D does not fall below v_G by more than V_{tn} → pinch-offed channel at the drain



$NMOS\ i_D - v_{DS}$ Characteristics

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor

- $\upsilon_{GS} < V_{tn}$: no channel ; transistor in cut-off; $i_D = 0$
- $\upsilon_{GS} = V_{tn} + \upsilon_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region

Continuous channel, obtained by:

$$\upsilon_{GD} > V_{tn}$$

or equivalently:

$$\upsilon_{DS} < \upsilon_{OV}$$

Then

$$i_D = k_n'\left(\frac{W}{L}\right)\left[\left(\upsilon_{GS} - V_{tn}\right)\upsilon_{DS} - \frac{1}{2}\upsilon_{DS}^2\right]$$

or equivalently

$$i_D = k_n'\left(\frac{W}{L}\right)\left(\upsilon_{OV} - \frac{1}{2}\upsilon_{DS}\right)\upsilon_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$\upsilon_{GD} \le V_{tn}$$

or equivalently:

$$\upsilon_{DS} \ge \upsilon_{OV}$$

Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\left(\upsilon_{GS} - V_{tn}\right)^2$$

or equivalently

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)\upsilon_{OV}^2$$

$i_D - v_{DS}$ Characteristics

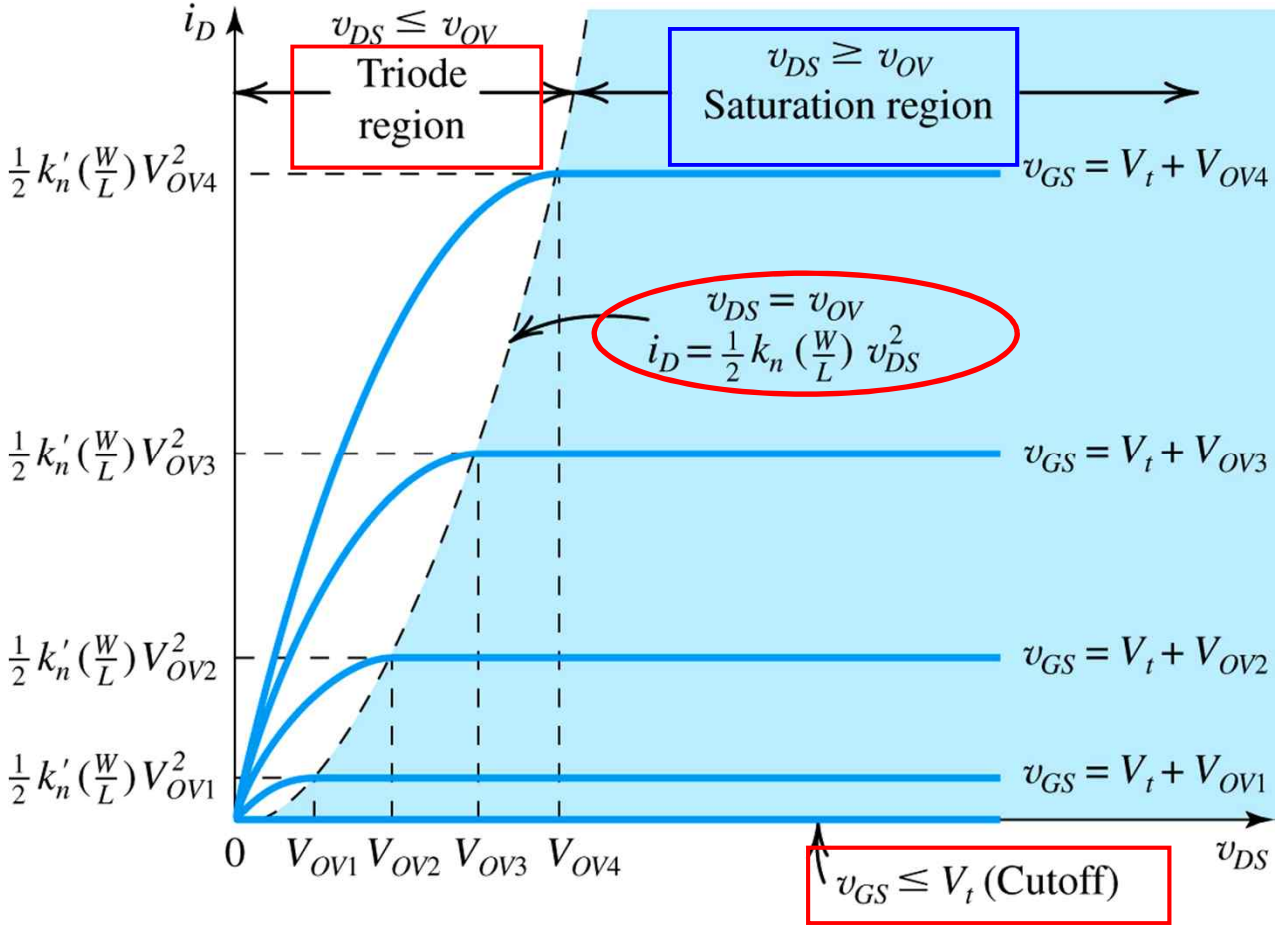


Figure 5.13 The i_D–v_{DS} characteristics for an enhancement-type NMOS transistor.

- v_{GS} above V_{tn} by V_{OV1}, V_{OV2}, V_{OV3} & V_{OV4}
- Saturation current i_D is directly determined by v_{OV} → $1/2k'_nV_{OV1}^2$, $1/2k'_nV_{OV2}^2$…
- Boundary between triode and saturation regions = locus of the saturation points
  → parabolic curve of

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{DS}^2$$

- In saturation, i_D is constant determined by v_{GS} (or v_{OV}) & is independent of v_{DS}

$i_D - v_{GS}$ Characteristic (*Saturation* region)

MOSFET as an amplifier →saturation region
→ Nonlinear voltage controlled current source

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v_{GS} - V_t)^2$$

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) v_{OV}{}^2$$

BJT as an amplifier →active region
→ Nonlinear voltage controlled current source

$$i_C = I_S e^{v_{BE}/V_T}$$

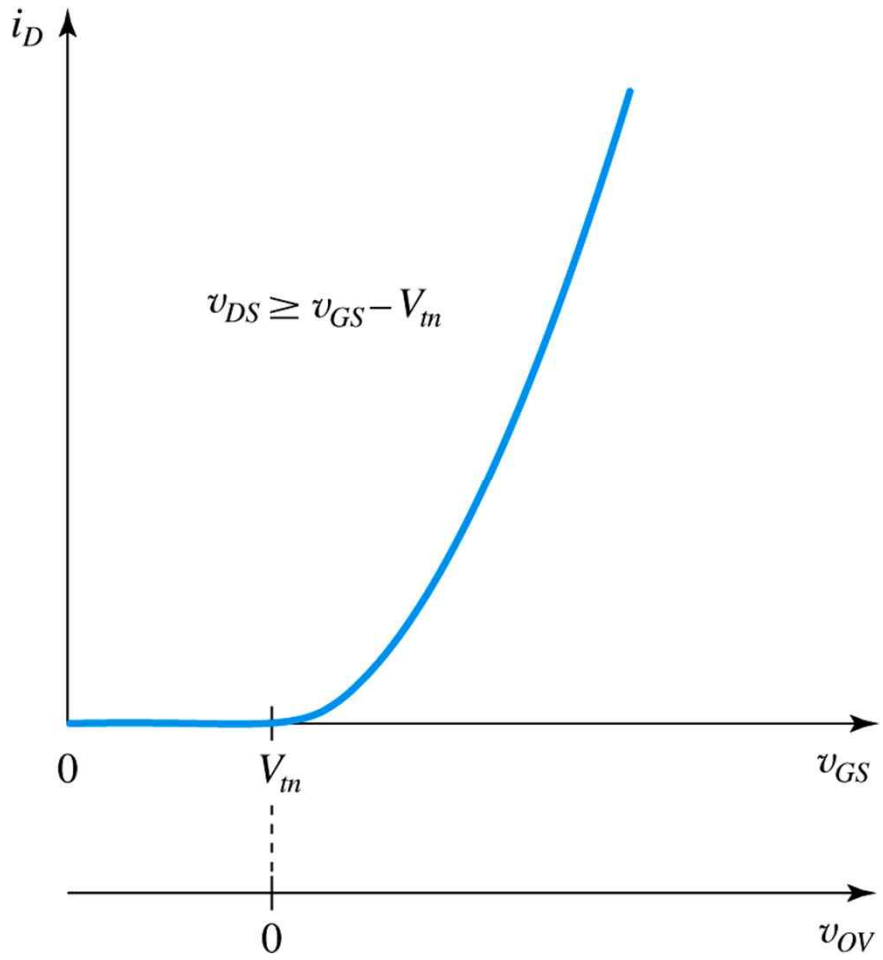
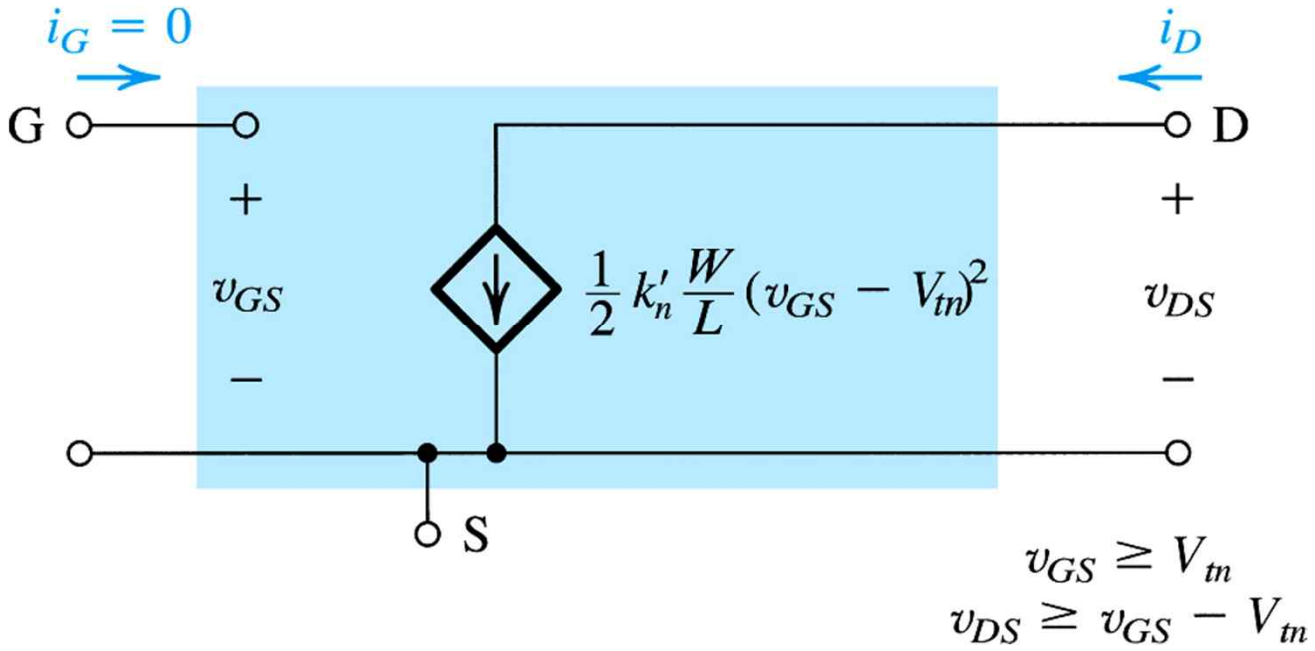


Figure 5.14 The i_D–v_{GS} characteristic of an NMOS transistor operating in the saturation region. The i_D–v_{OV} characteristic can be obtained by simply re-labelling the horizontal axis; that is, shifting the origin to the point $v_{GS} = V_{tn}$.

Large-Signal Equivalent-Circuit Model in the *Saturation* Region



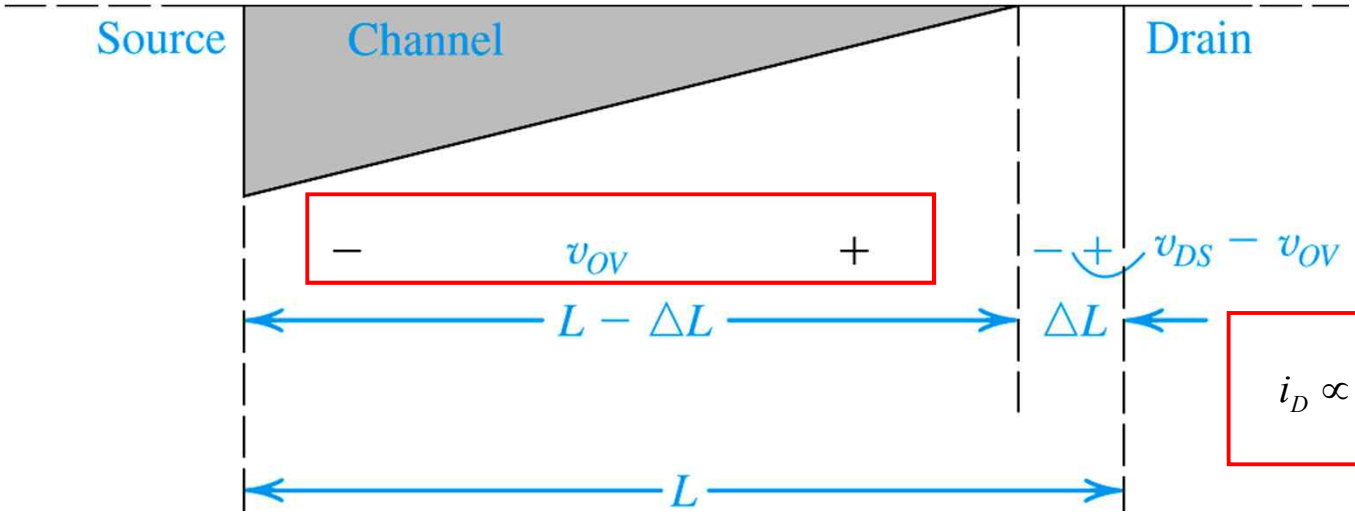
- The saturated MOSFET behaves as an ideal current source whose value is controlled by v_{GS} according to the below nonlinear relationship

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L} \right) (v_{GS} - V_t)^2$$

- Large signal equivalent circuit : ideal current source with infinite output resistance
  → i_D is independent from v_{DS}

Finite Output Resistance in Saturation

- Ideal case : Infinite resistance in saturation → i_D is independent of v_{DS} → once channel is pinched off at the drain end, further increase in v_{DS} have *no effect on the channel's shape*
- practical case :
  - As v_{DS} is increased beyond v_{OV}, the channel pinch-off point is moved slightly away from the drain, toward the source.
  - Voltage *across the channel* remains constant at v_{OV}
  - The additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of channel and the drain region
  - The voltage, "v_{DS} - v_{OV}" accelerates the electrons that reach the end of the channel and sweeps them across the depletion region into the drain.
    → channel length modulation (L reduces to $L - \Delta L$)



The effective channel length is reduced by ΔL

$$i_D \propto \frac{1}{L} \rightarrow i_D \uparrow \quad when \quad v_{DS} \uparrow, L \downarrow$$

Finite Output Resistance in Saturation

- i_D - v_{DS} w/ channel length modulation

$$i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

- *Linear dependence* of i_D on v_{DS} in the *saturation region* by the factor of $1+\lambda v_{DS}$
- Output resistance is *not infinite*

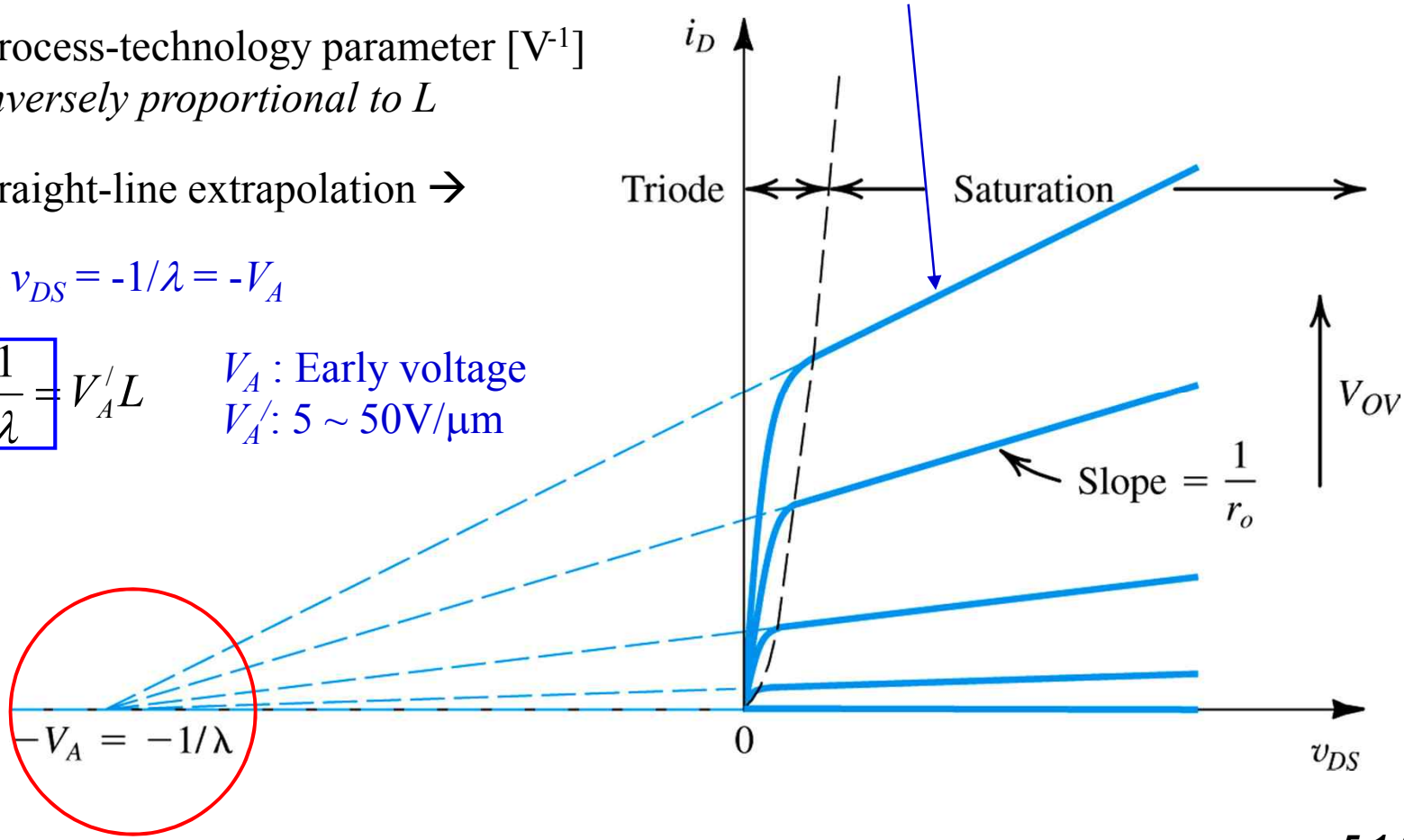
λ : process-technology parameter [V^{-1}]
inversely proportional to L

- $i_D - v_{DS}$ straight-line extrapolation →

$i_D = 0$ at $v_{DS} = -1/\lambda = -V_A$

$$V_A = \frac{1}{\lambda} = V_A' L$$

V_A : Early voltage
V_A': 5 ~ 50V/μm



Large-Signal Equivalent-Circuit Model in Saturation Region

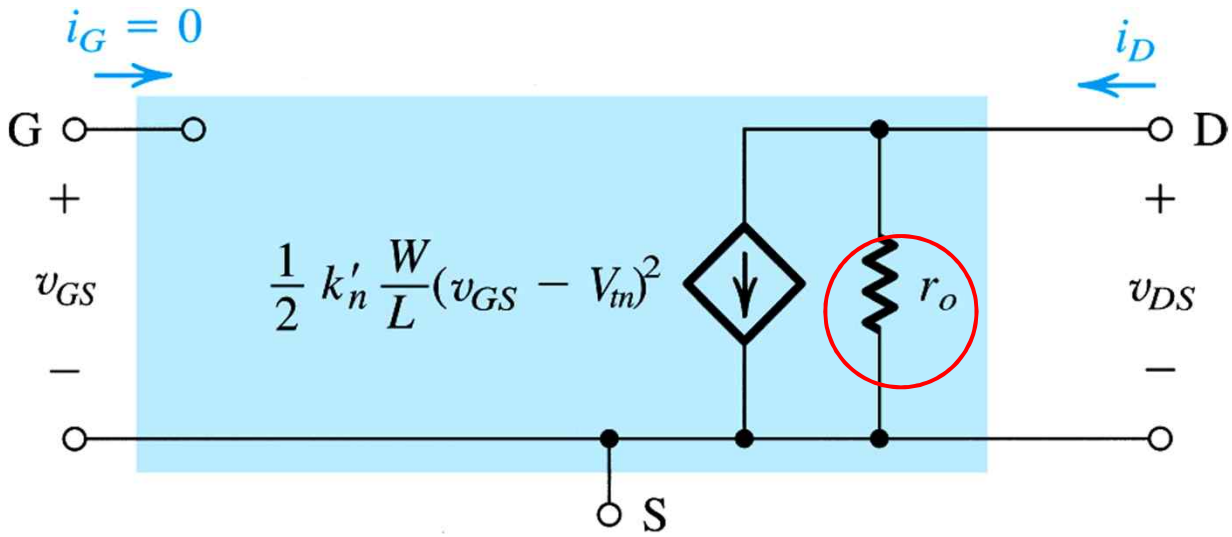
- Output resistance

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\ constant} = \left[\lambda \frac{1}{2} k_n' \frac{W}{L}(v_{GS} - V_t)^2\right]^{-1} = \frac{1}{\lambda I_D} = \boxed{\frac{V_A}{I_D}}$$

$$where \quad I_D = \frac{1}{2} k_n' \frac{W}{L}(V_{GS} - V_t)^2$$

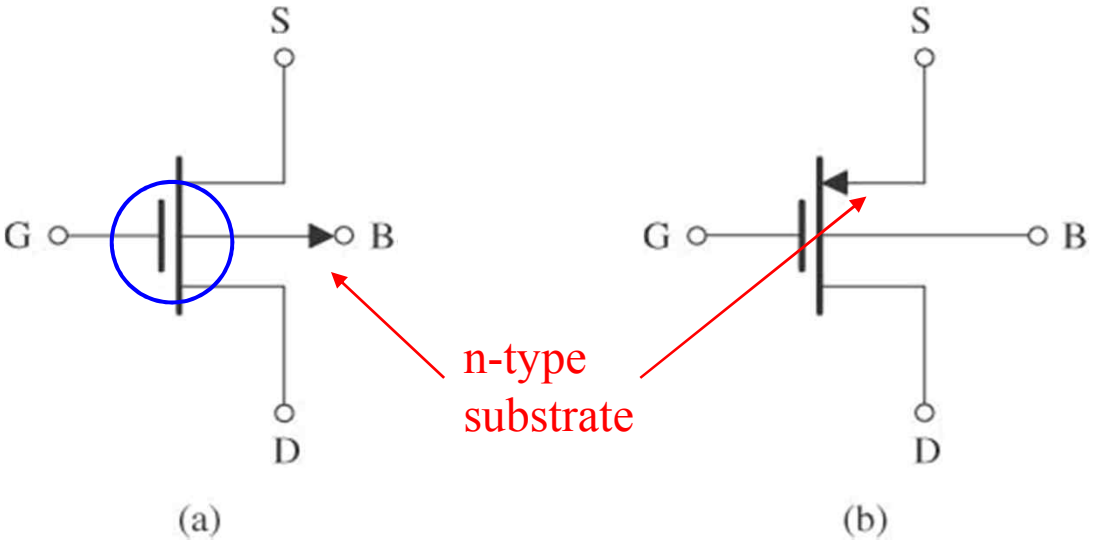
Drain current w/o channel-length modulation taken into account

Output resistance is *inversely* proportional to the drain current & *finite*

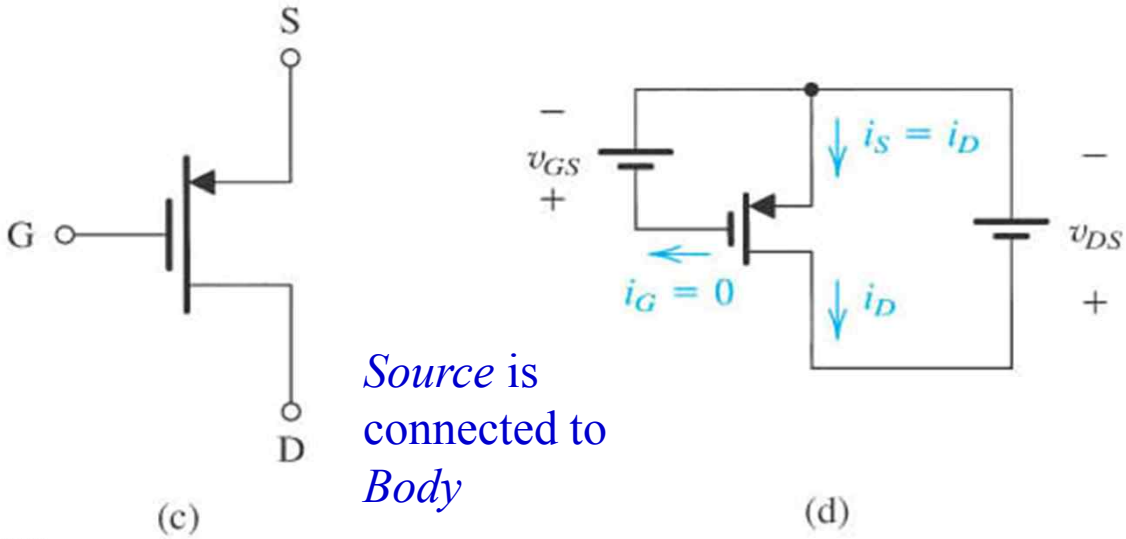


r_O models the linear dependence of i_D on v_{DS}

p-Channel MOSFET



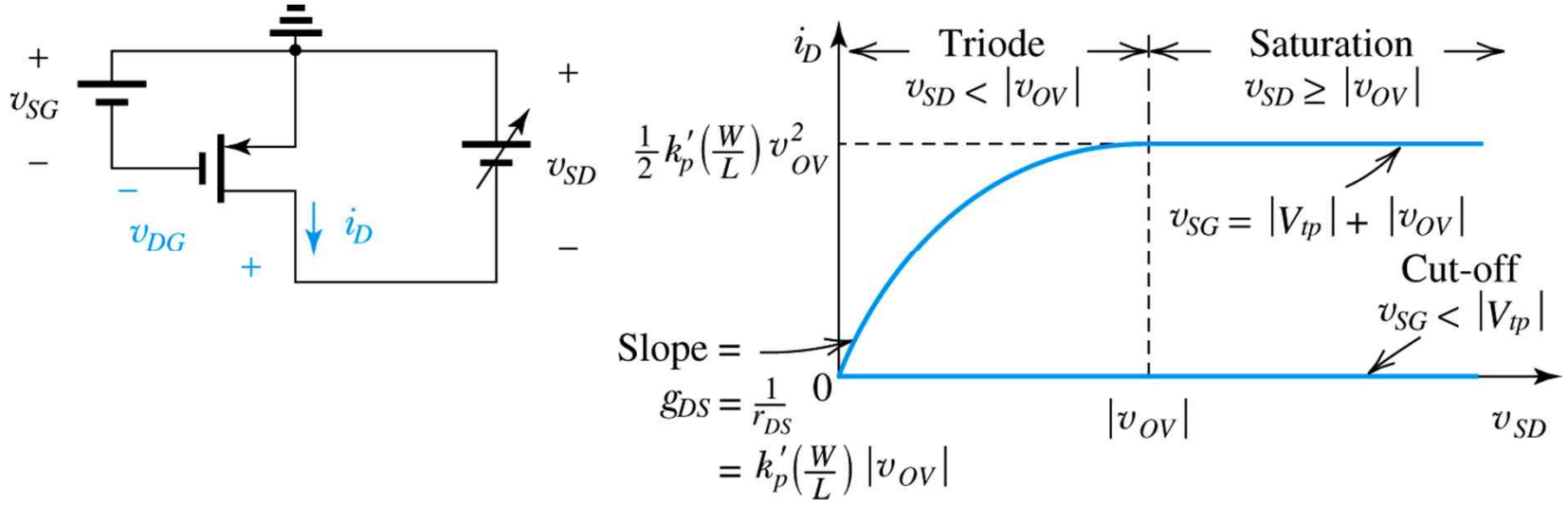
- n-type substrate
- arrowhead : normal direction of current flow
- threshold voltage $V_{tp} < 0$



Source is connected to *Body*

$v_{GS} < 0$, $v_{DS} < 0$
i_D flow out of D
p-channel devices w/ sources on top so that current flows from top to bottom

p-Channel MOSFET



- $V_{tp} < 0$, $v_{SG} > 0$, $v_{SD} > 0$
- Saturation region w/ channel-length modulation effect (λ, $V_A < 0$)

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)\left(v_{SG} - |V_{tp}|\right)^2\left(1 + |\lambda| v_{SD}\right) = \frac{1}{2}k_p'\left(\frac{W}{L}\right)\left(v_{SG} - |V_{tp}|\right)^2\left(1 + \frac{v_{SD}}{|V_A|}\right)$$

PMOS $i_D - v_{DS}$ Characteristics

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor

$\upsilon_{SG} < |V_{tp}|$: no channel ; transistor in cut-off; $i_D = 0$

- $\upsilon_{SG} = |V_{tp}| + |\upsilon_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region

Continuous channel, obtained by:

$$\upsilon_{DG} > V_{tp}$$

or equivalently:

$$\upsilon_{SD} < |\upsilon_{OV}|$$

Then

$$i_D = k_p'\left(\frac{W}{L}\right)\left[\left(\upsilon_{SG} - |V_{tp}|\right)\upsilon_{SD} - \frac{1}{2}\upsilon_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|\upsilon_{OV}| - \frac{1}{2}\upsilon_{SD}\right)\upsilon_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$\upsilon_{DG} \leq |V_{tp}|$$

or equivalently:

$$\upsilon_{SD} \geq |\upsilon_{OV}|$$

Then

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)\left(\upsilon_{SG} - |V_{tp}|\right)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)\upsilon_{OV}^2$$

i_D in Triode and Saturation Regions

In triode region

$$v_{GS} \le V_{tp} \quad or \quad v_{SG} \ge |V_{tp}| \qquad (Induced \ \ channel)$$

$$v_{DS} \ge v_{GS} - V_t \quad (v_{GS}, V_{tp}, v_{DS} < 0) \qquad (Continuous \ \ channel)$$

$$i_D = k_p' \frac{W}{L}\left[(v_{GS} - V_{tp})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

drain voltage must be higher than gate voltage by at least $|V_t|$

$$where \ \ k_p' = \mu_p C_{ox}$$

μ_p: mobility of holes in the induced p channel (μ_p = 0.25~0.5μ_n)

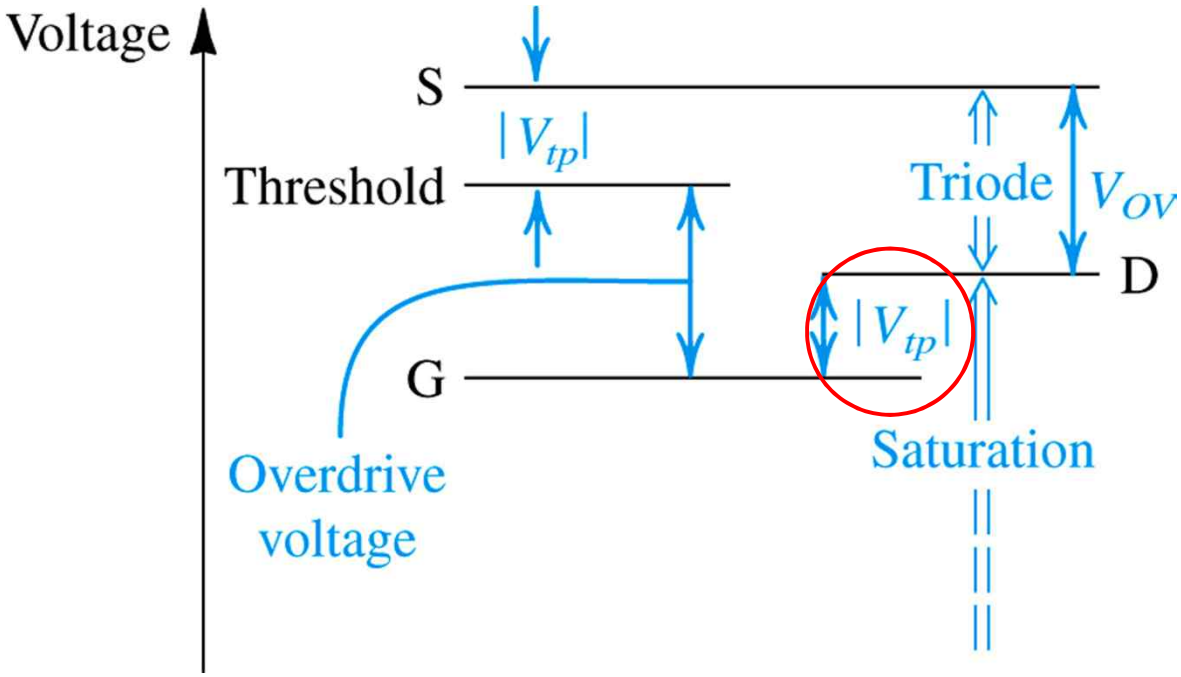
In saturation region

$$v_{DS} \le v_{GS} - V_{tp} \quad (v_{GS}, V_{tp}, v_{DS}, \lambda < 0) \qquad (Pinched-off \ \ channel)$$

$$i_D = \frac{1}{2}k_p' \frac{W}{L}(v_{GS} - V_{tp})^2(1 + \lambda v_{DS})$$

drain voltage must be lower than gate voltage by at least $|V_t|$

Relative Levels of Terminal Voltages for PMOS



Triode region : drain voltage must be higher than gate voltage by at least $|V_{tp}|$

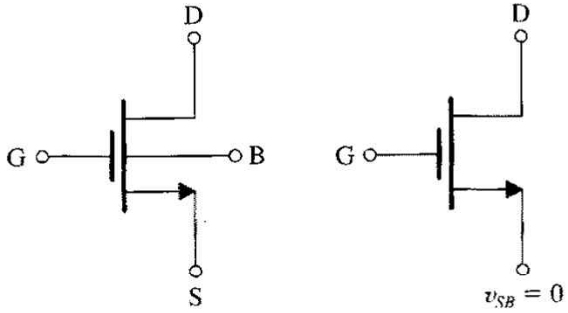
Saturation region : drain voltage must be lower than gate voltage by at least $|V_t|$

To turn PMOS on, gate voltage has to be made lower than source voltage by at least $|V_{tp}|$
To operate in the triode region, the drain voltage has to exceed that of the gate by at least $|V_{tp}|$; otherwise, the PMOS operates in saturation

TABLE 4.1 Summary of the MOSFET Current-Voltage Characteristics

NMOS Transistor

Symbol:



Overdrive voltage:

$$v_{OV} = v_{GS} - V_t$$

$$v_{GS} = V_t + v_{OV}$$

Operation in the *triode* region:

- Conditions:

  (1) $v_{GS} \geq V_t \quad \Leftrightarrow \quad v_{OV} \geq 0$

  (2) $v_{GD} \geq V_t \quad \Leftrightarrow \quad v_{DS} \leq v_{GS} - V_t \quad \Leftrightarrow \quad v_{DS} \leq v_{OV}$

- i-v Characteristics:

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

- For $v_{DS} \ll 2(v_{GS} - V_t) \quad \Leftrightarrow \quad v_{DS} \ll 2v_{OV}$

$$r_{DS} \equiv \frac{v_{DS}}{i_D} = 1\Big/\left[\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)\right]$$

Operation in the *saturation* region:

- Conditions:

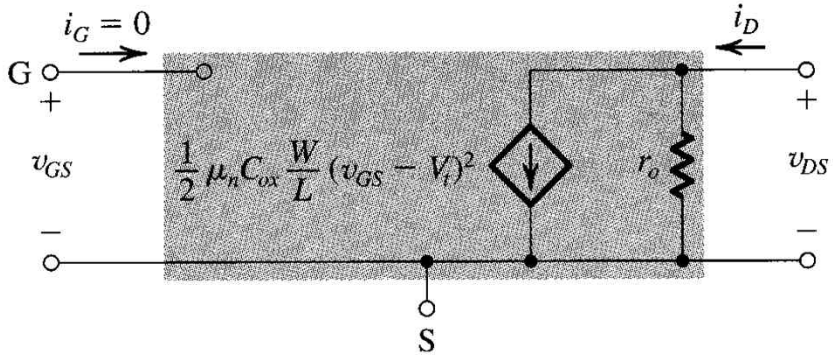
  (1) $v_{GS} \geq V_t \quad \Leftrightarrow \quad v_{OV} \geq 0$

  (2) $v_{GD} \leq V_t \quad \Leftrightarrow \quad v_{DS} \geq v_{GS} - V_t \quad \Leftrightarrow \quad v_{DS} \geq v_{OV}$

- i-v Characteristics:

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

- Large-signal equivalent circuit model:



$$r_o = \left[\lambda \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2\right]^{-1} = \frac{V_A}{I_D}$$

where

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Threshold voltage:

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f})$$

Process parameters:

$C_{ox} = \varepsilon_{ox}/t_{ox}$	(F/m^2)
$k_n' = \mu_n C_{ox}$	(A/V^2)
$V_A' = (V_A/L)$	(V/m)
$\lambda = (1/V_A)$	(V^{-1})
$\gamma = \sqrt{2qN_A\varepsilon_s}/C_{ox}$	$(\text{V}^{1/2})$

Constants:

$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.45 \times 10^{-11}$ F/m

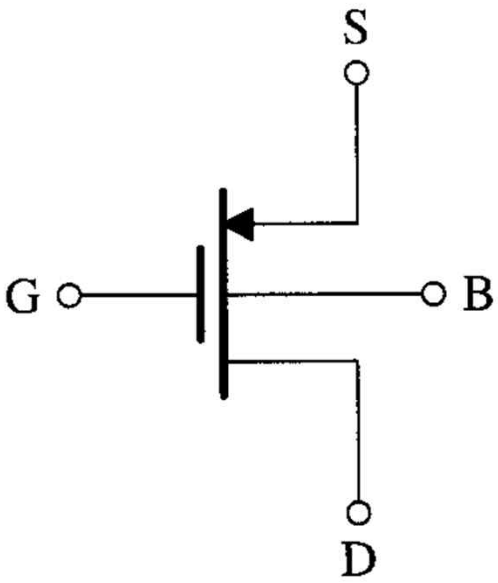
$\varepsilon_s = 11.7\varepsilon_0 = 1.04 \times 10^{-10}$ F/m

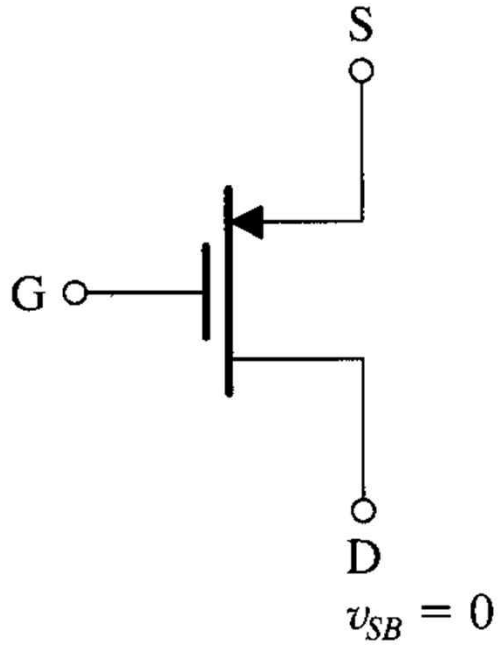
$q = 1.602 \times 10^{-19}$ C

Summary

PMOS Transistor

Symbol:





$v_{SB} = 0$

Overdrive voltage:

$$v_{OV} = v_{GS} - V_t$$

$$v_{SG} = |V_t| + |v_{OV}|$$

***i-v* Characteristics:**

Same relationships as for NMOS transistors except:

- Replace μ_n, k_n', and N_A with μ_p, k_p', and N_D, respectively.
- V_t, V_{t0}, V_A, λ, and γ are negative.
- Conditions for operation in the **triode** region:

  (1) $v_{GS} \le V_t \quad \Leftrightarrow \quad v_{OV} \le 0 \quad \Leftrightarrow \quad v_{SG} \ge |V_t|$

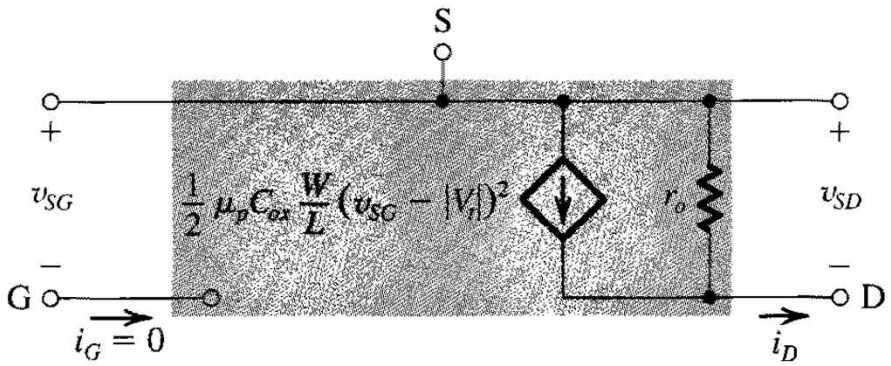
  (2) $v_{DG} \ge |V_t| \quad \Leftrightarrow \quad v_{DS} \ge v_{GS} - V_t \quad \Leftrightarrow \quad v_{SD} \le |v_{OV}|$

- Conditions for operation in the **saturation** region:

  (1) $v_{GS} \le V_t \quad \Leftrightarrow \quad v_{OV} \le 0 \quad \Leftrightarrow \quad v_{SG} \ge |V_t|$

  (2) $v_{DG} \le |V_t| \quad \Leftrightarrow \quad v_{DS} \le v_{GS} - V_t \quad \Leftrightarrow \quad v_{SD} \ge |v_{OV}|$

- Large-signal equivalent circuit model:



$$r_o = \left[|\lambda|\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG} - |V_t|)^2\right]^{-1} = \frac{|V_A|}{I_D}$$

where

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG} - |V_t|^2)$$